

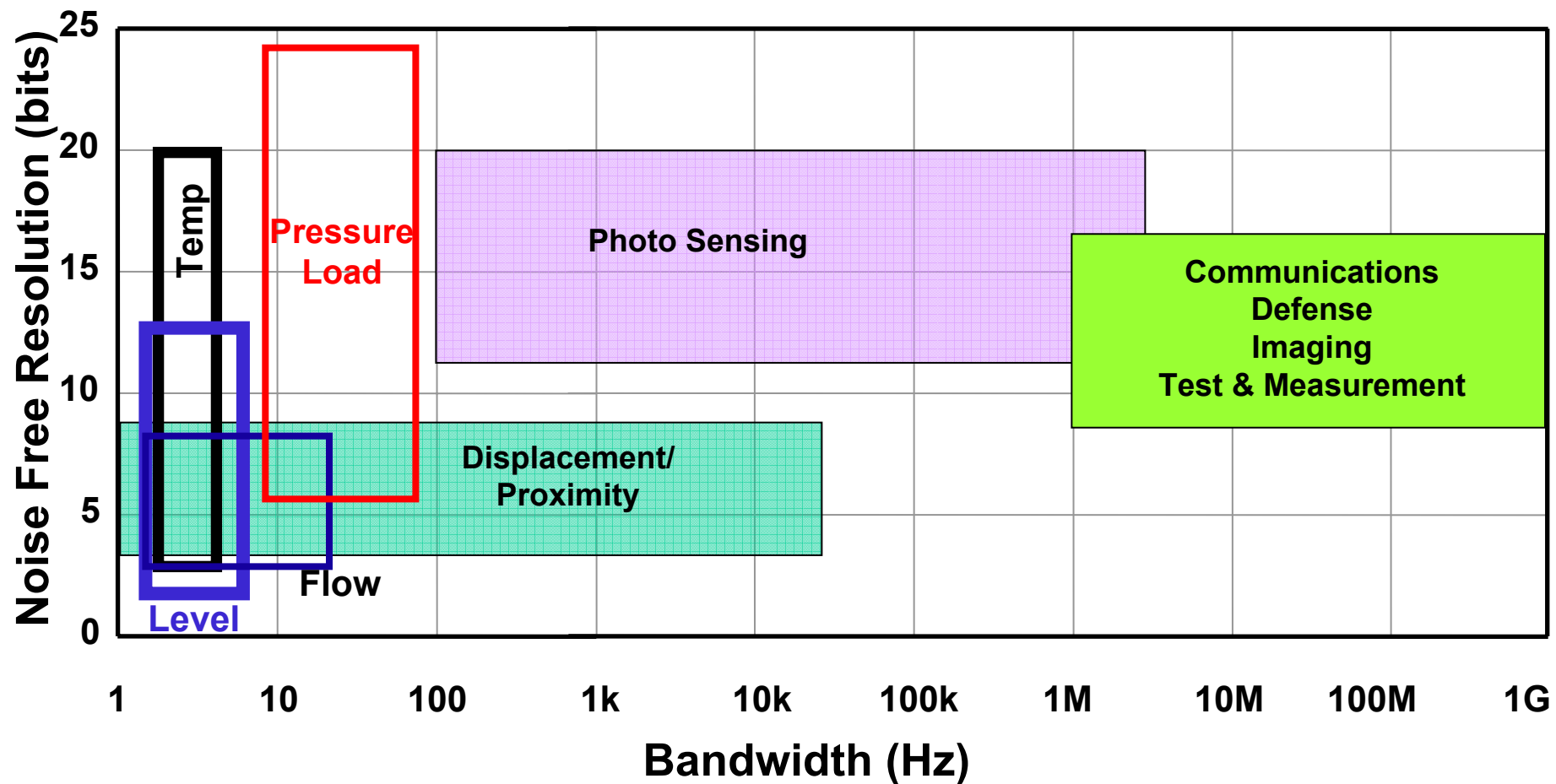
**Choose the right A/D converter
for your application**

Agenda

- Analog-to-Digital-Converters (ADCs)
 - What are the Signal Frequencies
 - Analog Classes of applications
 - Frequency ranges of ADCs
 - Nuts and Bolts of Delta-Sigma Converters
 - The SAR ADC
 - The High-speed Pipeline Topology

- Digital-to-Analog-Converters (DACs)
 - R-2R-DACs
 - String-DACs
 - Multiplying DACs
 - Delta-Sigma DACs
 - High-Speed Current-Steering DACs

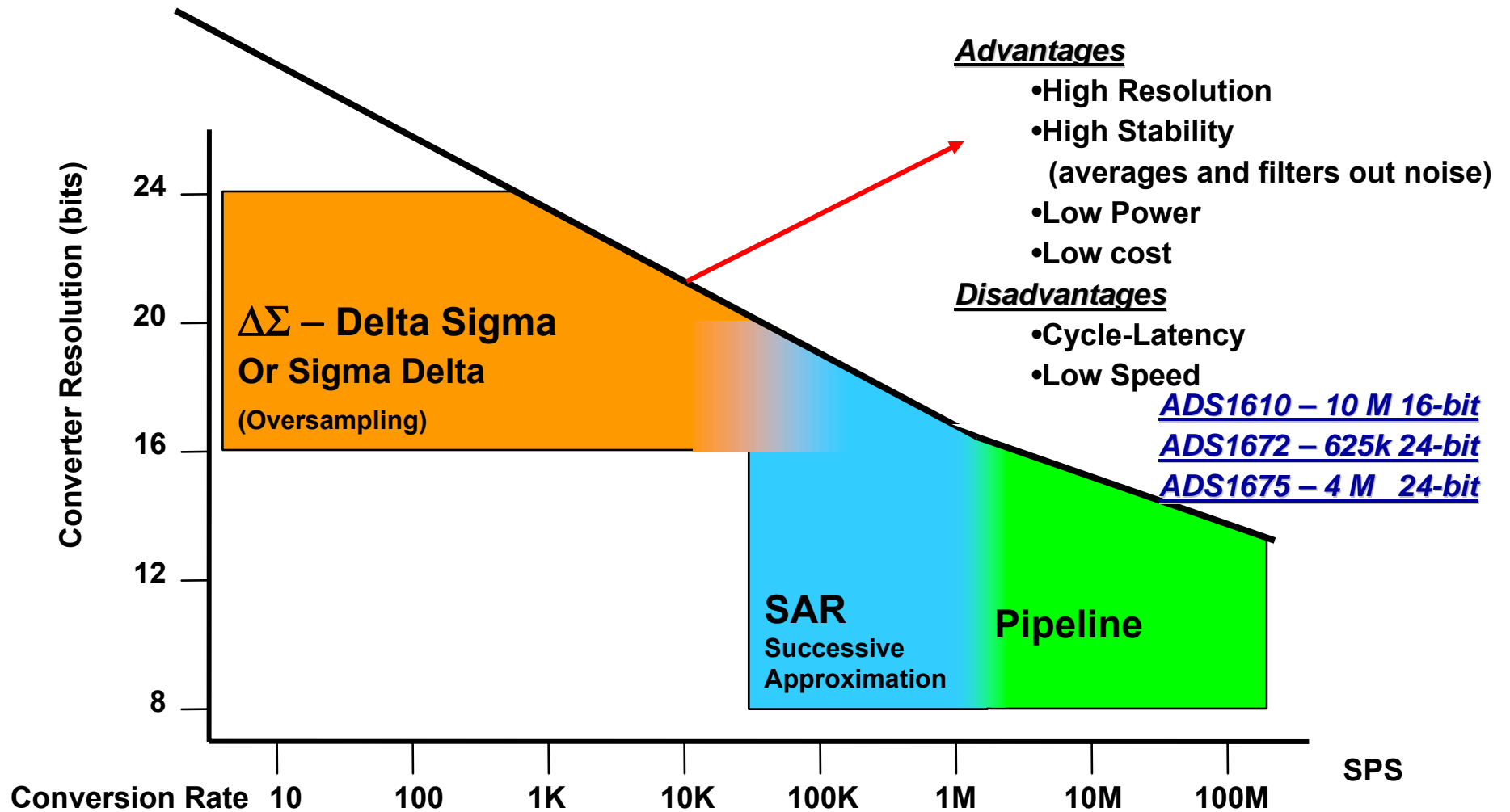
Real World vs. Bandwidth



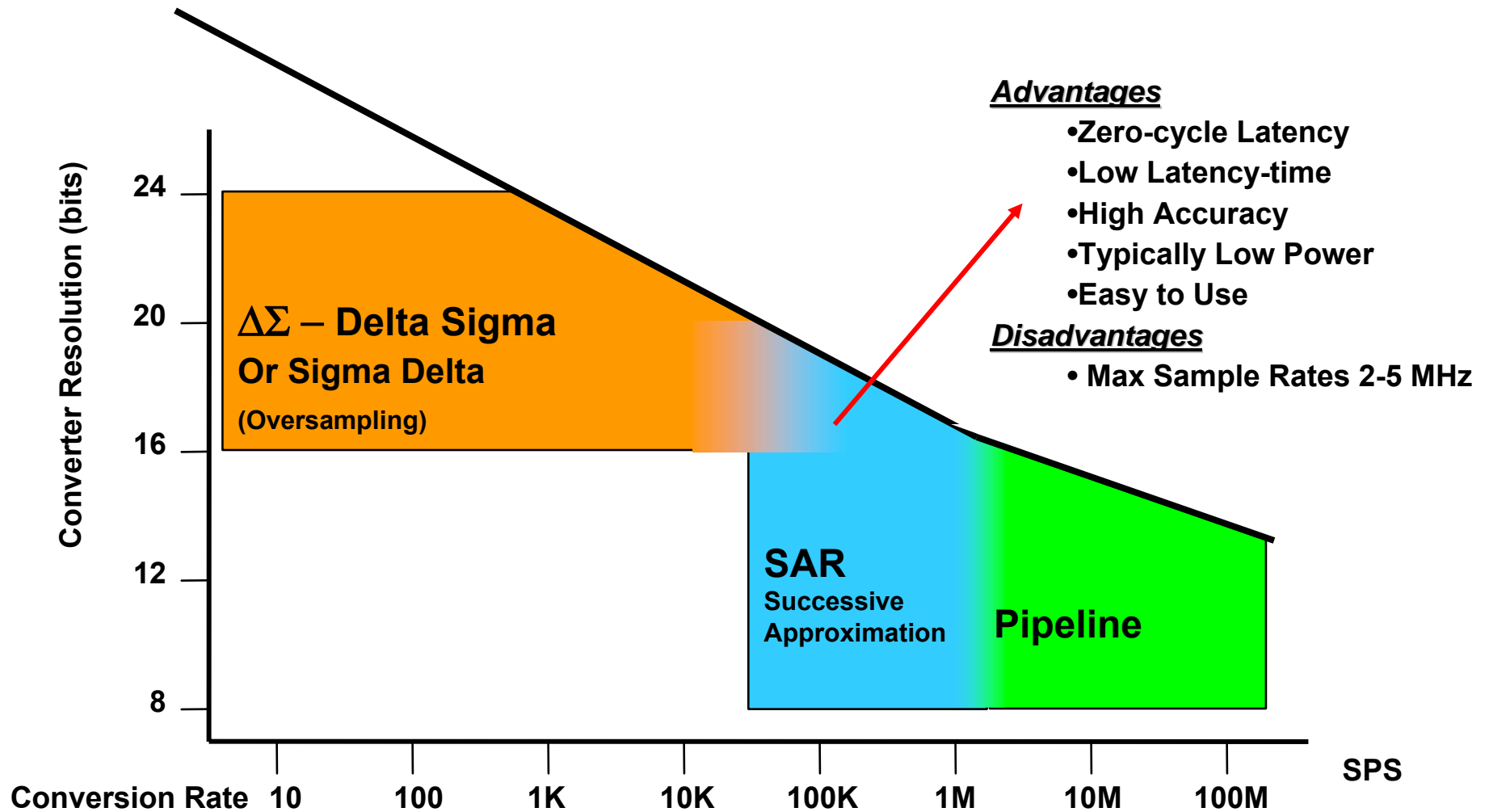
ADC Architectures

- **There are many different ADC Architectures**
 - **Successive Approximation (SAR)**
 - **Delta-Sigma ($\Delta\Sigma$)**
 - **Pipeline**
 - **(Flash)**
- **Delta-Sigma converters determine the digital word by**
 - **Oversampling**
 - **Applying Digital Filtering**
- **SARs determine the digital word by**
 - **Sampling the input signal**
 - **Using an iterative process**
- **Pipeline converters determine digital word by**
 - **Undersampling**
 - **With Sample / Gain Algorithm Topology**
 - **Multiple stages / Larger Cycle-latency**

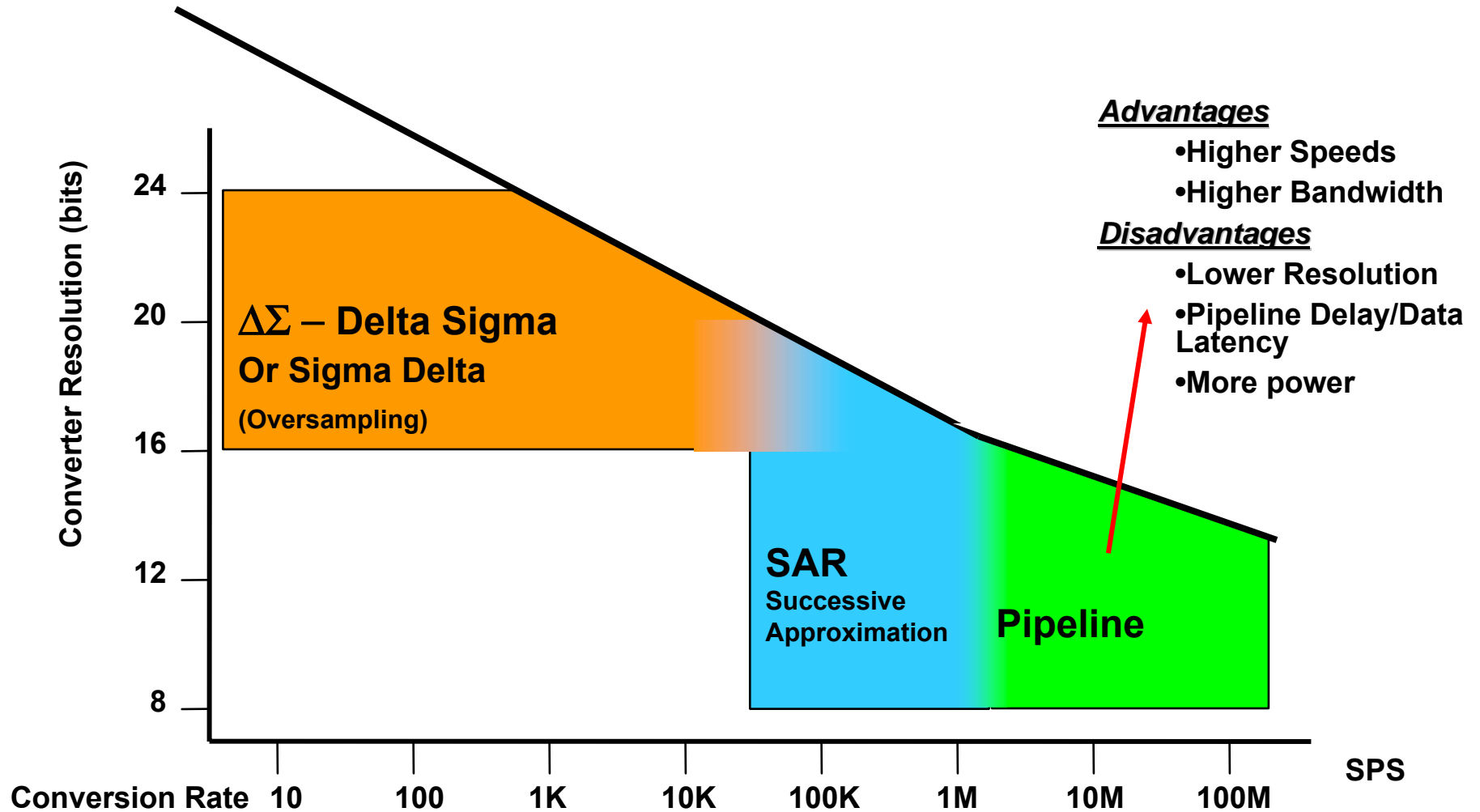
ADC Technologies - $\Delta\Sigma$



ADC Technologies - SAR



ADC Technologies - pipeline



Selecting ADC Topology

<i>ADC Topology</i>	<i>F Conversion</i>	<i>Resolution</i>	<i>Comments</i>
SAR	$\leq 4\text{Msps}$ $\leq 1.25\text{Msps}$	$\leq 16\text{-bit}$ $\leq 18\text{-bit}$	Simple operation, low cost, low power.
Delta-Sigma	$\leq 4\text{ksps}$ $\leq 4\text{Msps}$ $\leq 10\text{Msps}$	$\leq 31\text{-bit}$ $\leq 24\text{-bit}$ $\leq 16\text{-bit}$	Moderate cost.
Pipeline	$\leq 200\text{Msps}$ $\leq 250\text{Msps}$ $\leq 550\text{Msps}$	$\leq 16\text{-bit}$ $\leq 14\text{-bit}$ $\leq 12\text{-bit}$	Fast, expensive, higher power requirements.

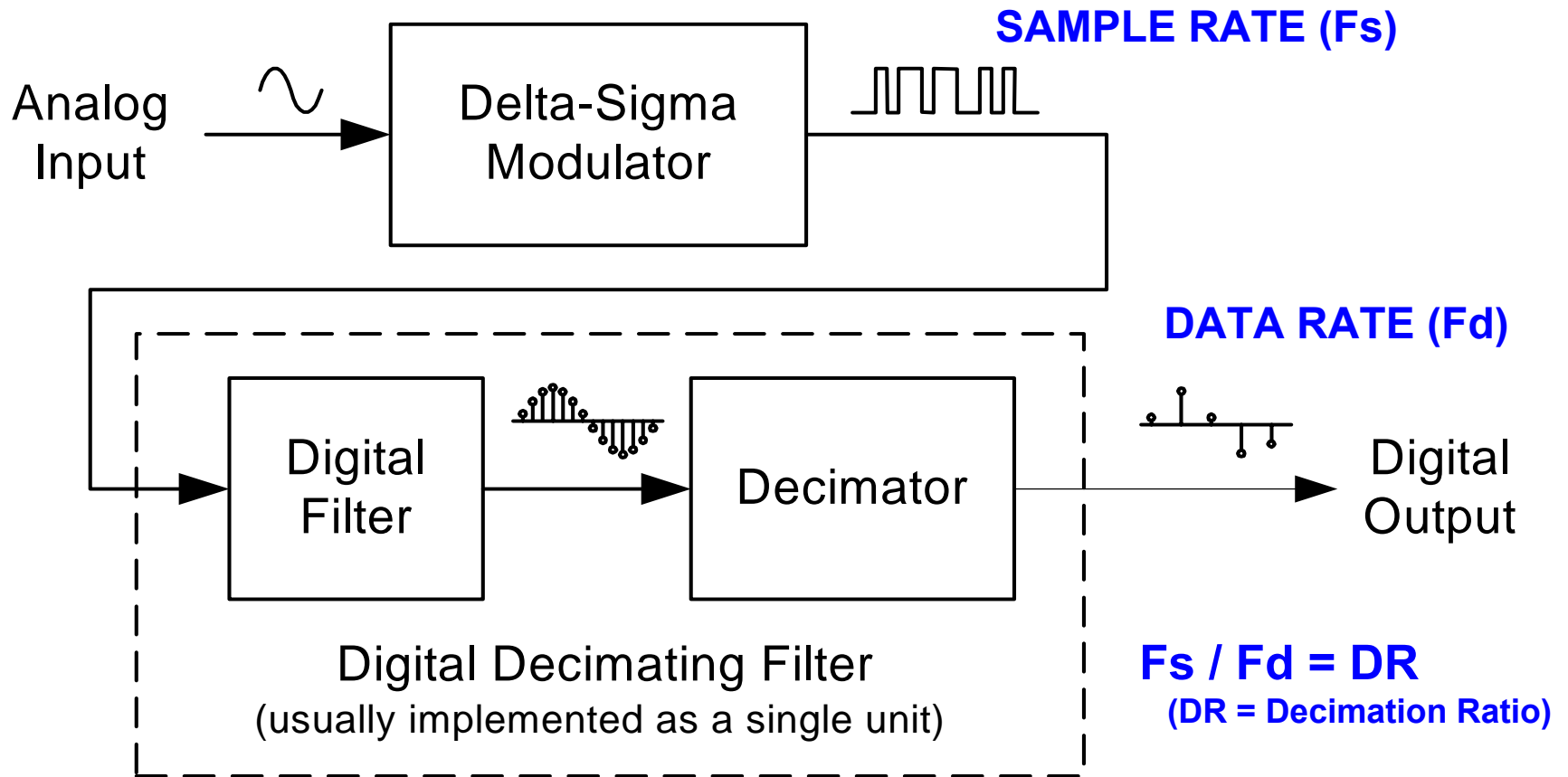
Which ADC Architecture to Use??

Characteristic	Pipelined	SAR	Delta Sigma
Throughput (samples/sec)	++	+	0/+
Resolution (ENOB)	0	+	++
Latency (Sample-to-Output)	+	++	0
Suitability for converting Multiple Signals per ADC	+	++	0
Capability to convert non-periodic multiplexed signals	+	++	-
Power Consumption	Scales with Sample Rate or Constant	Scales with Sample Rate	Constant

Applications for $\Delta\Sigma$ Converters

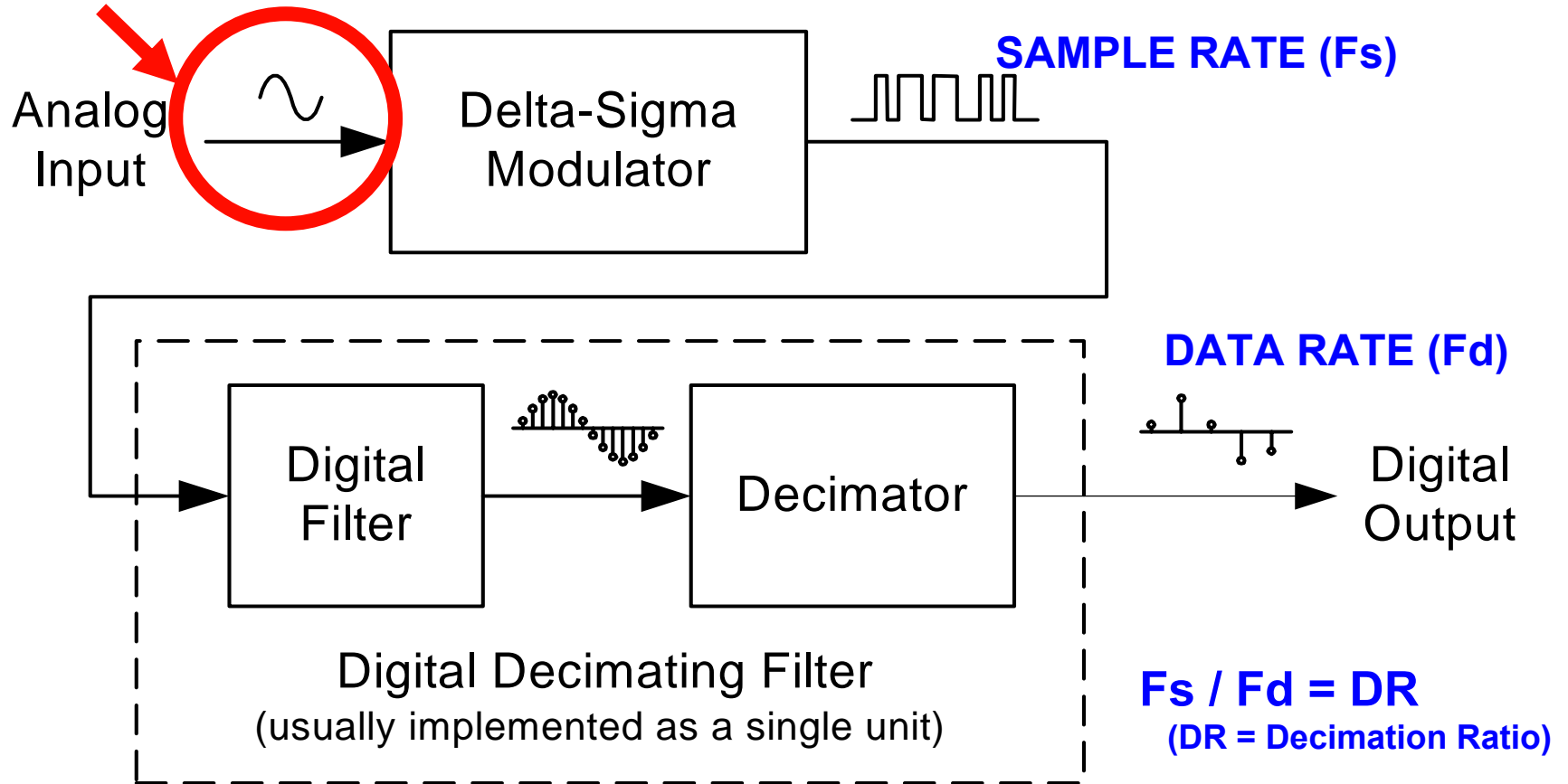
- Signal Level – System clock range ~ 0.5 to 40 MHz
 - Has an Internal Digital Low-Pass Filter
 - Uses an integrator
 - Accurate near DC
 - High Resolution – up to 24 bits
- Audio – System clock range ~ 20 to 40 MHz
 - Has an Internal Digital Low-Pass Filter
 - Optimized noise performance
 - Optimized filter in audio frequency for flatness

Delta-Sigma A/D Converters



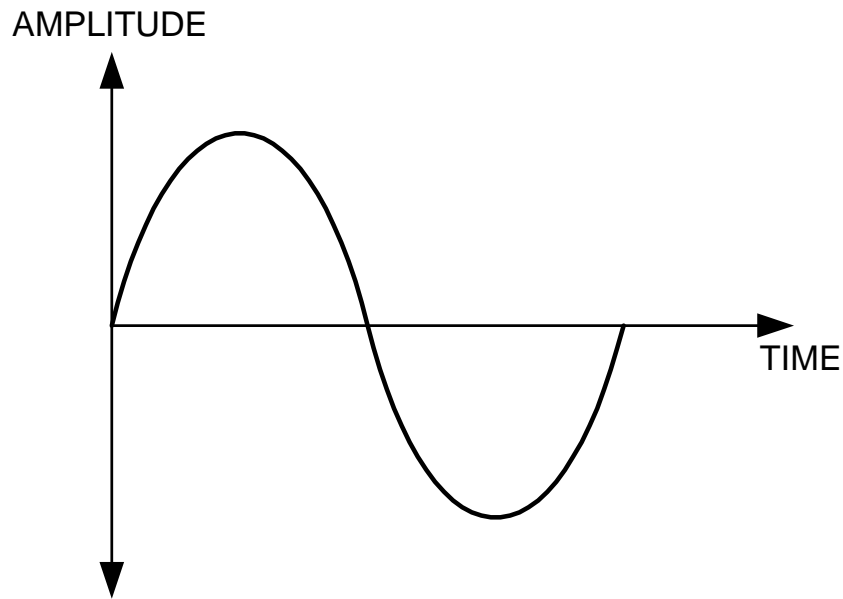
Input to the Delta-Sigma A/D

You are here

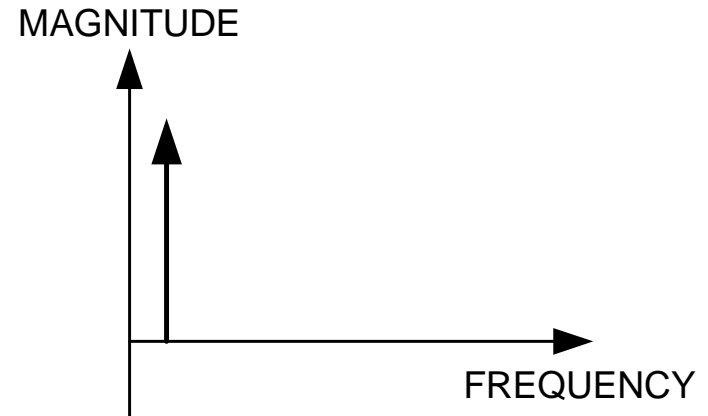


Input Signal

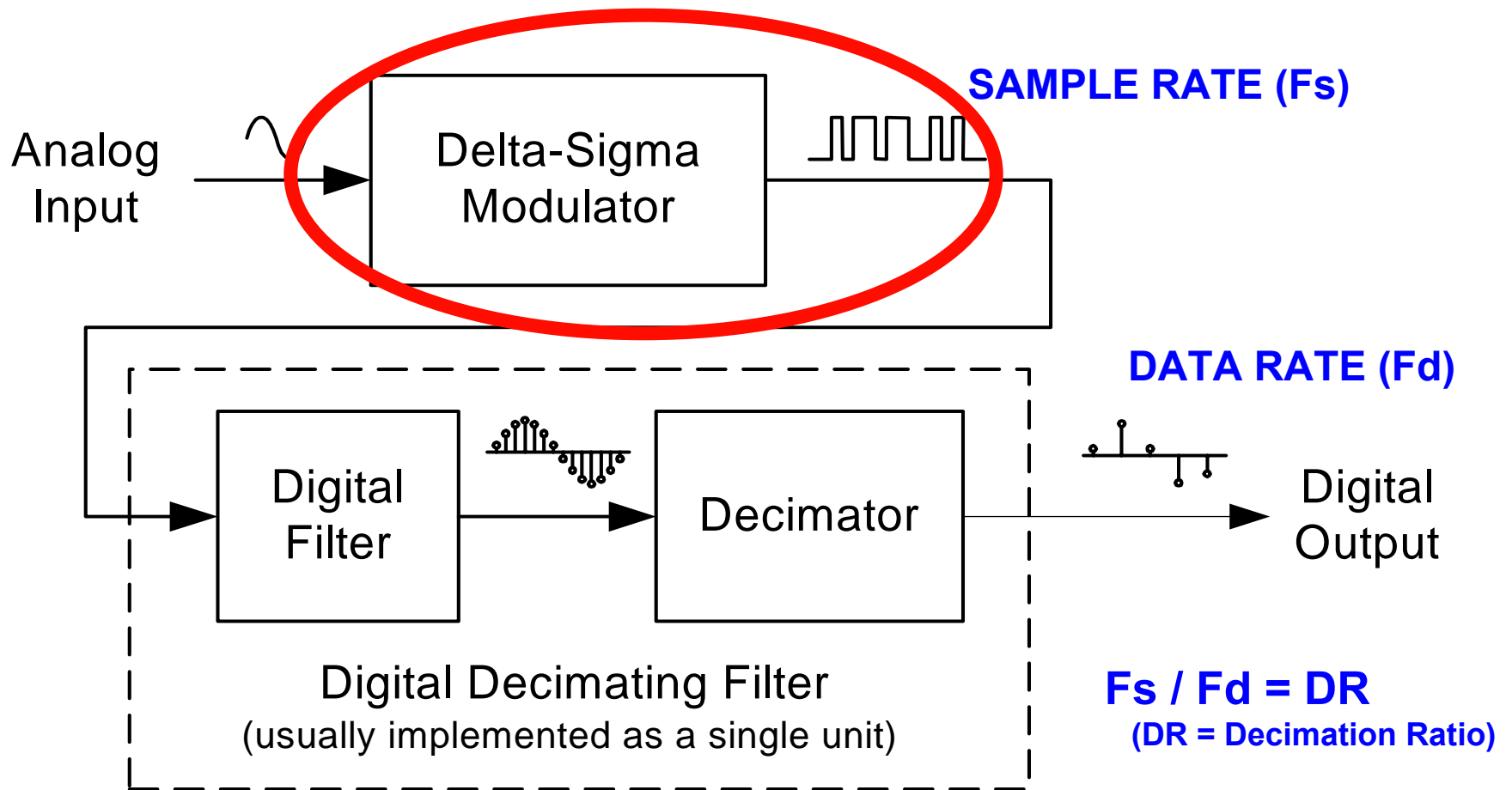
**Input Signal:
TIME DOMAIN**



**Input Signal:
FREQUENCY DOMAIN**

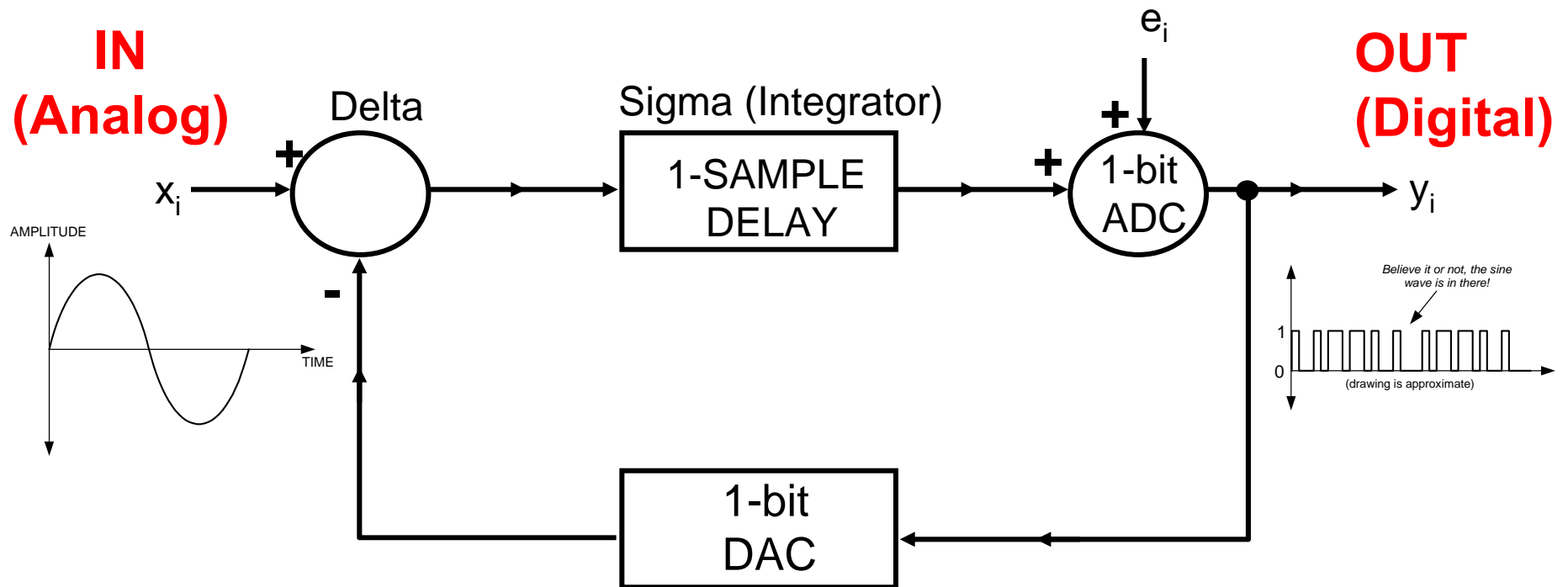


Modulator Output



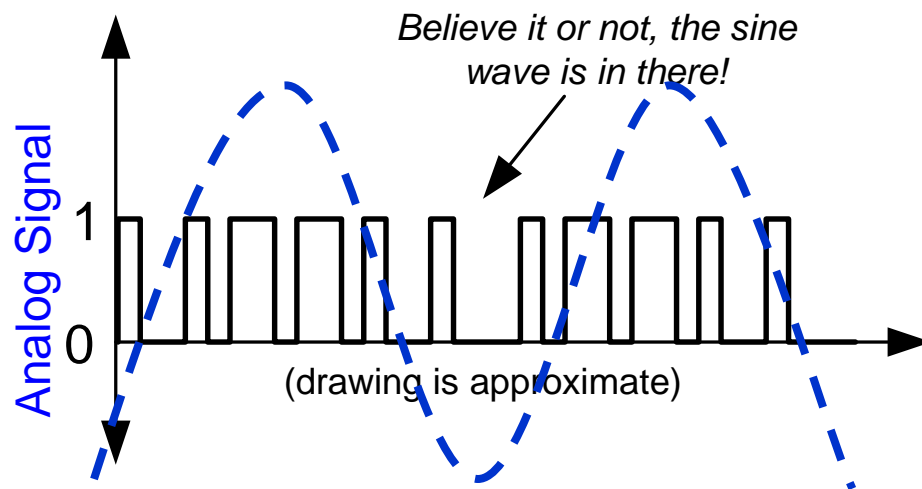
1st Order Delta-Sigma Modulator

TIME DOMAIN

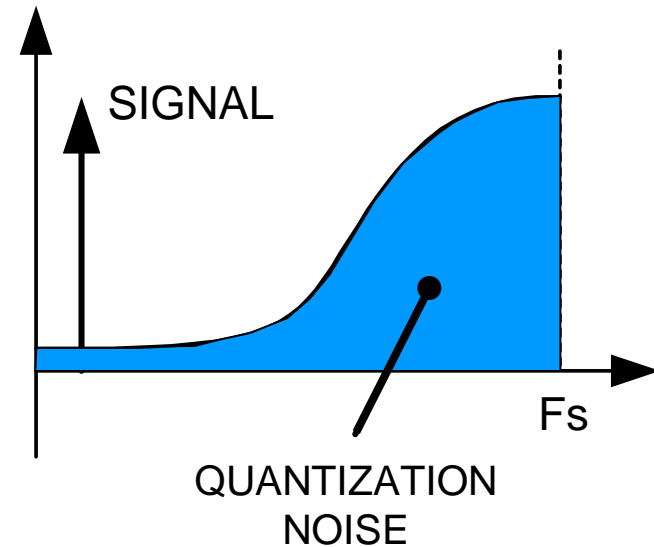


Modulator Output Signal

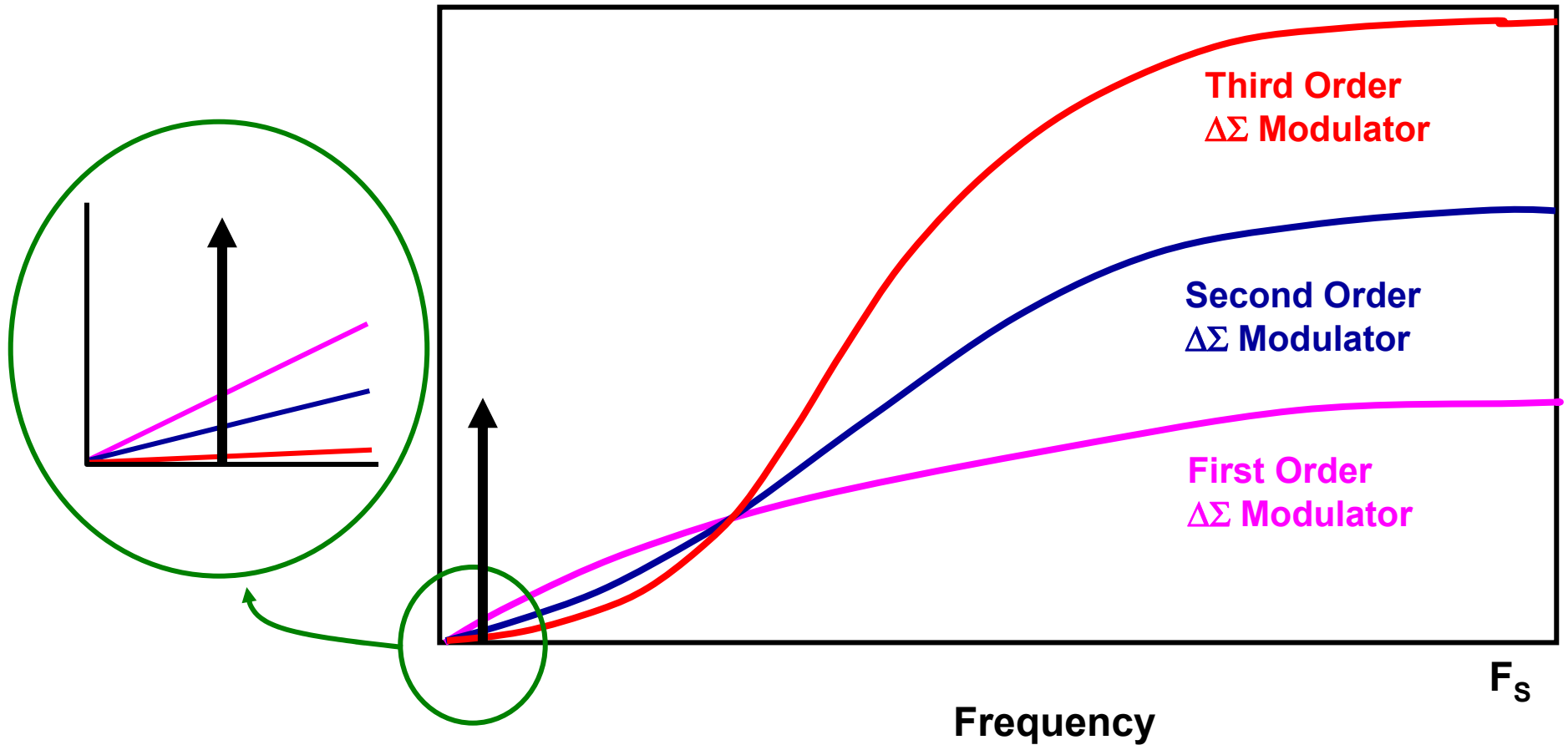
**Modulator Output:
TIME DOMAIN**



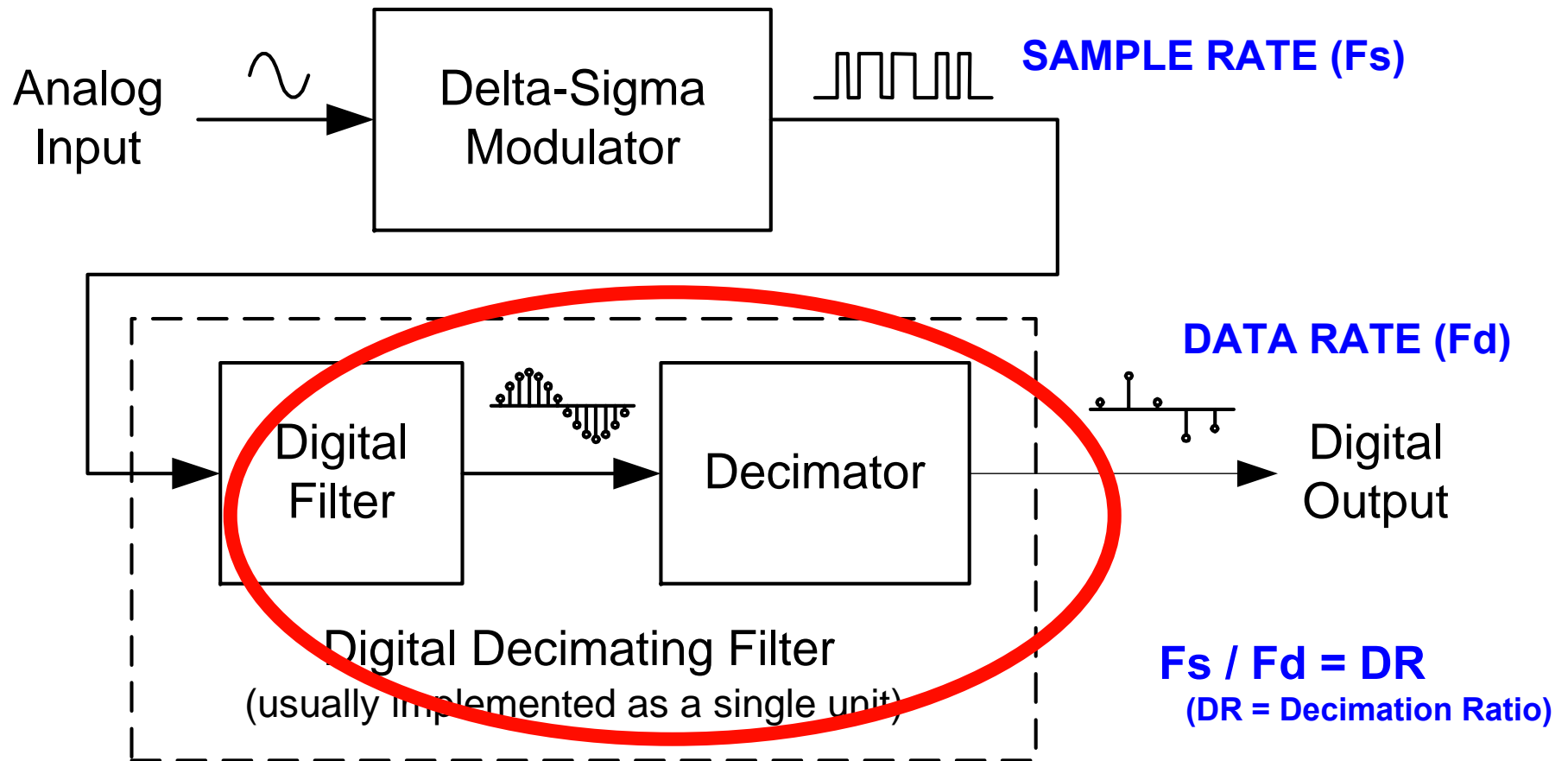
**Modulator Output:
FREQUENCY DOMAIN**



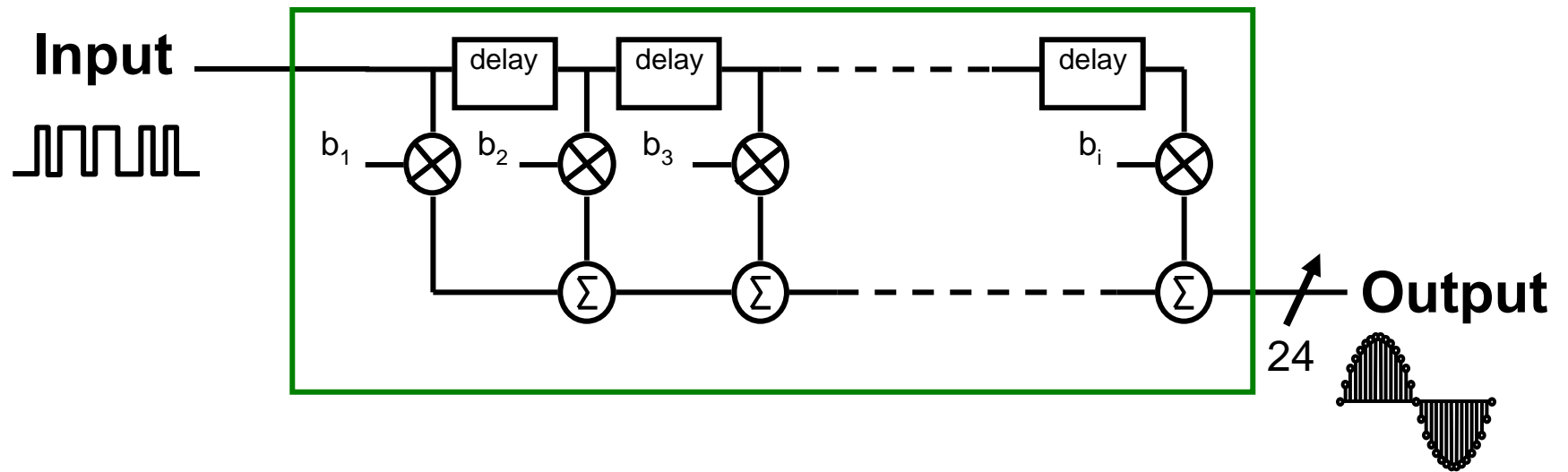
Multi-order Delta-Sigma Modulators



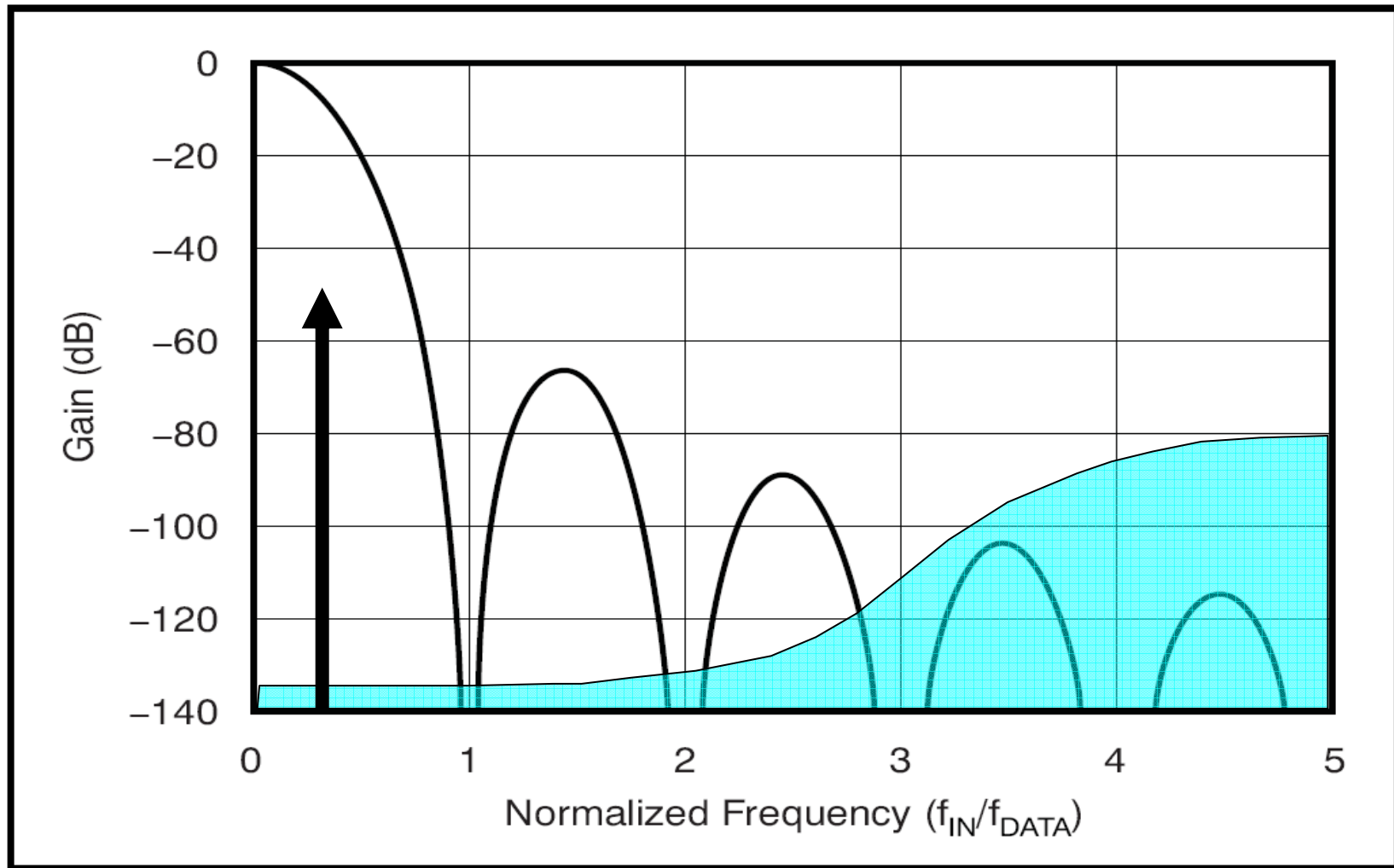
Delta-Sigma A/D Signal Path



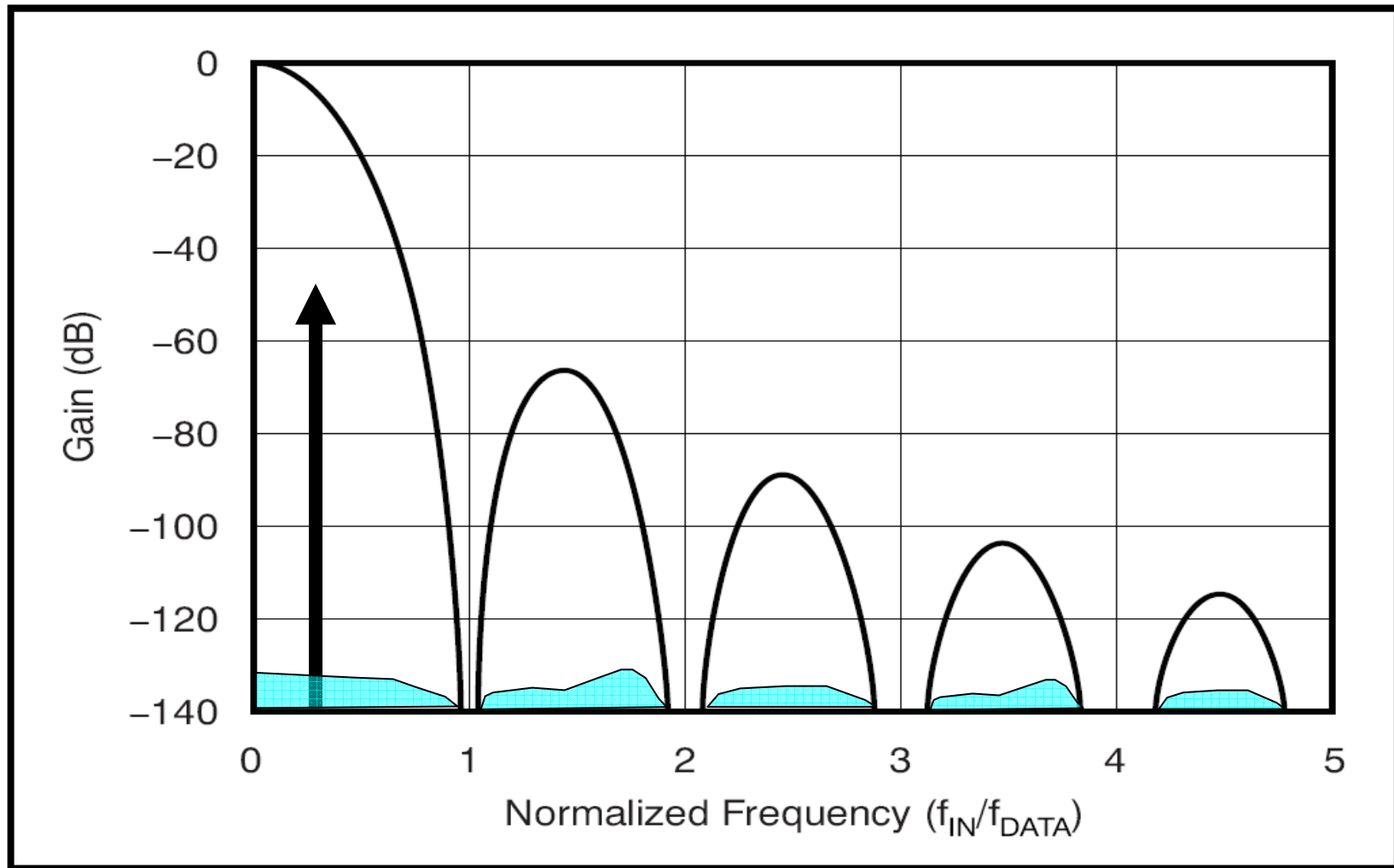
Digital Filter Function



High Frequency Noise Reduction

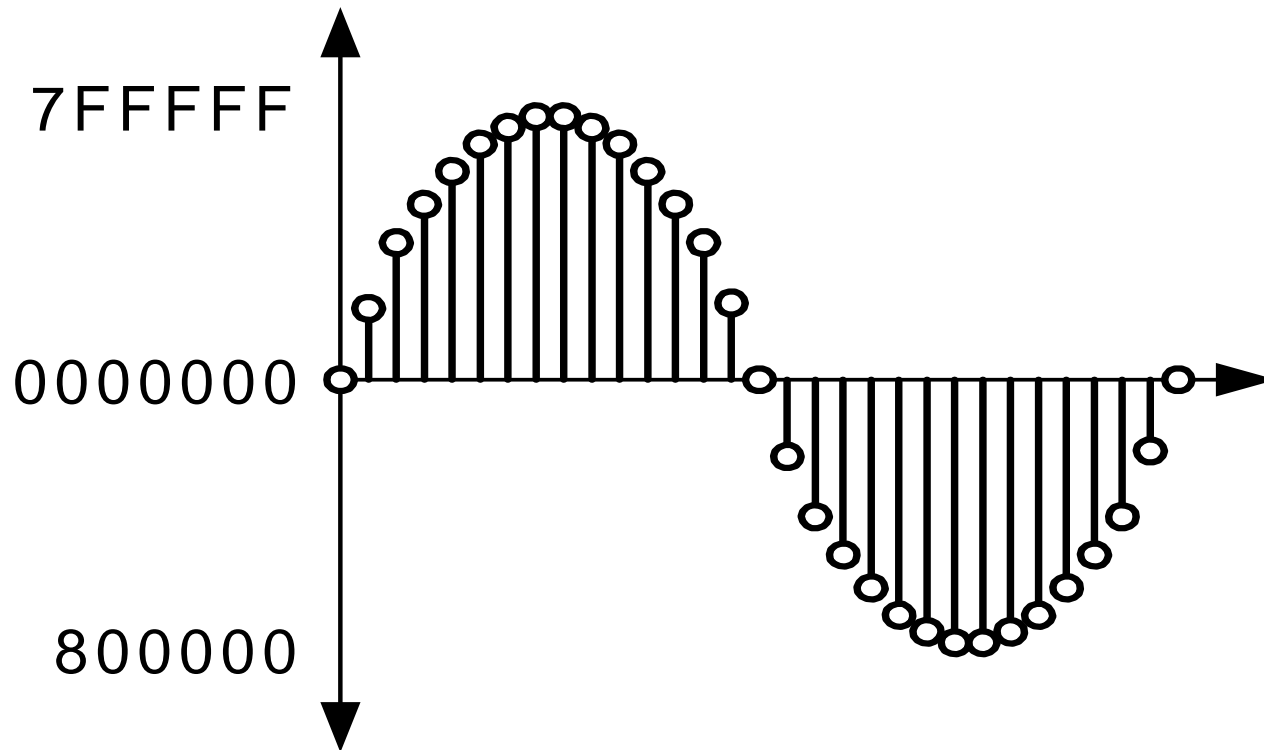


Sinc3 Filter response

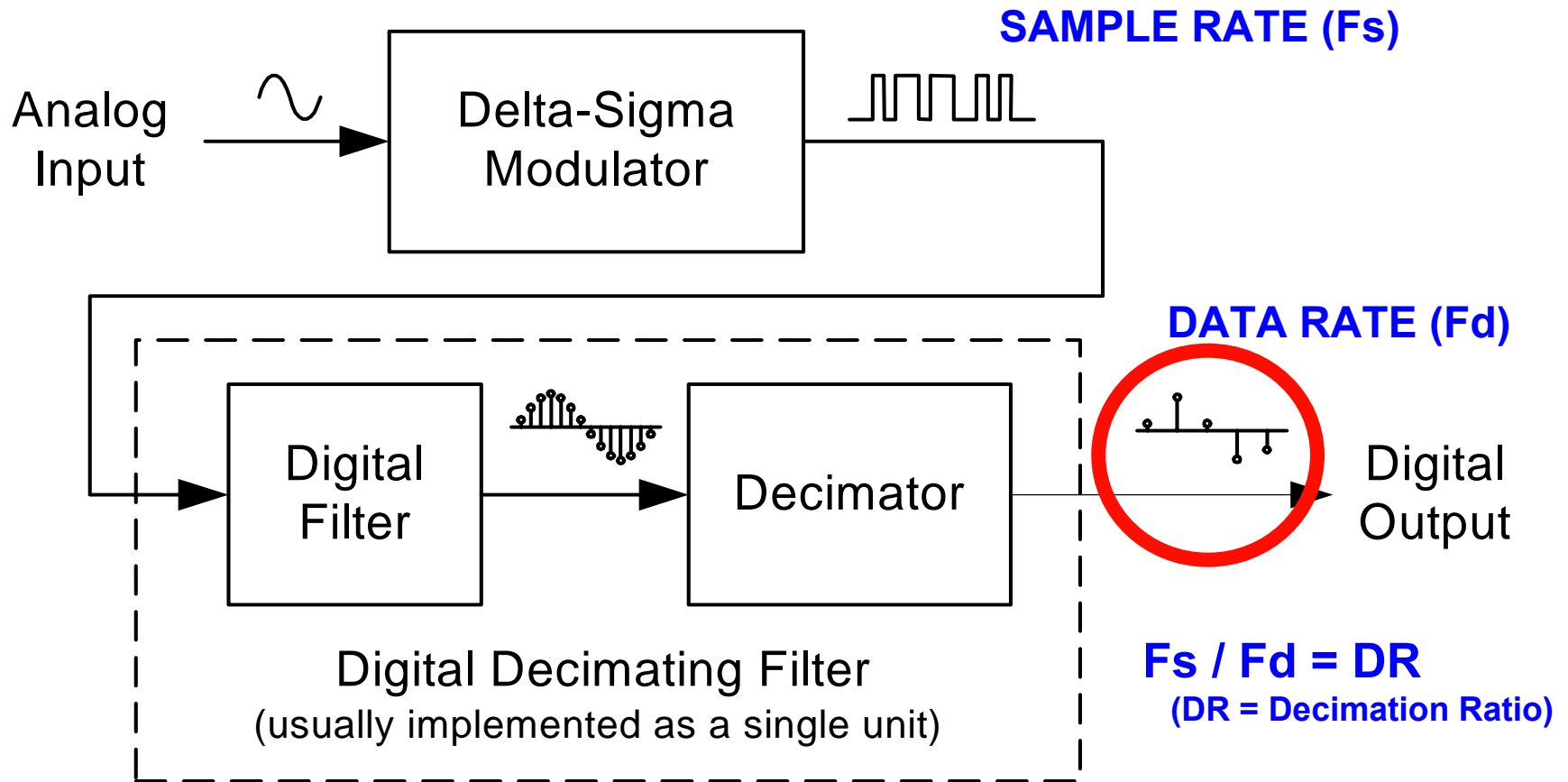


Outcome of Digital Filter Function

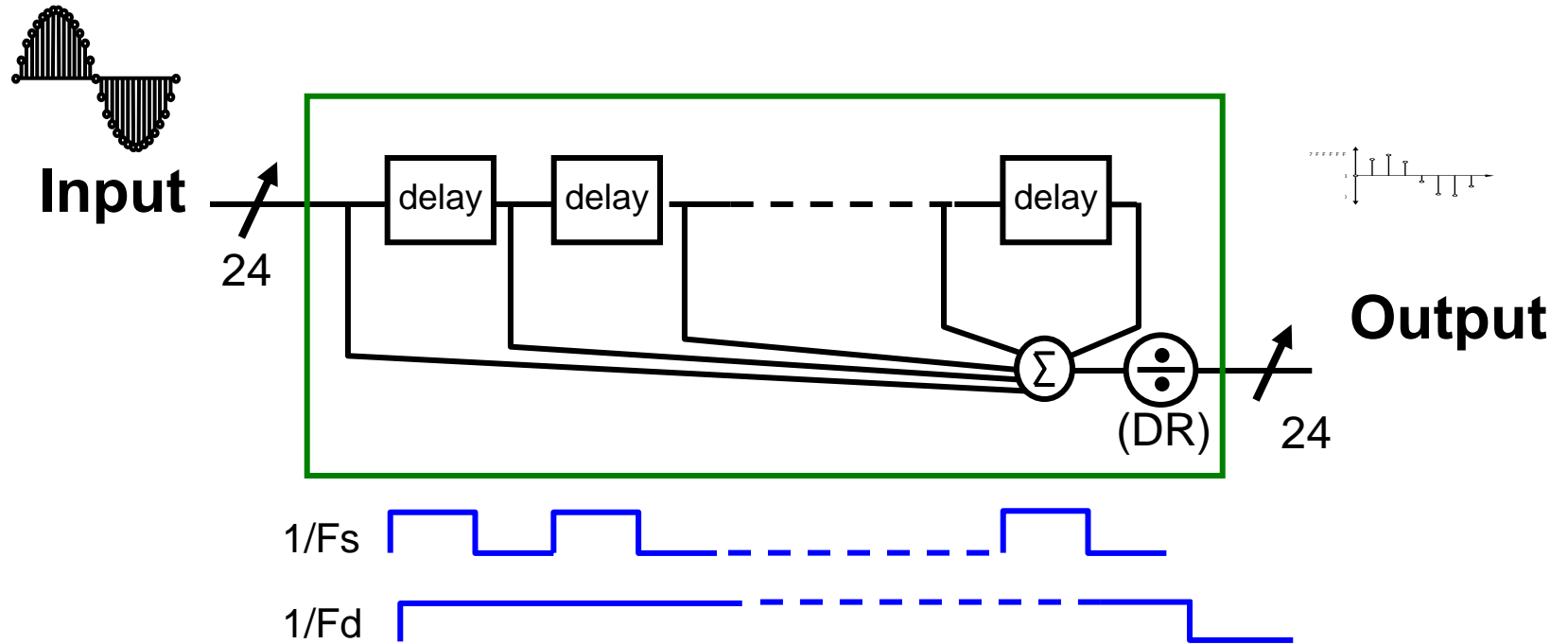
TIME DOMAIN



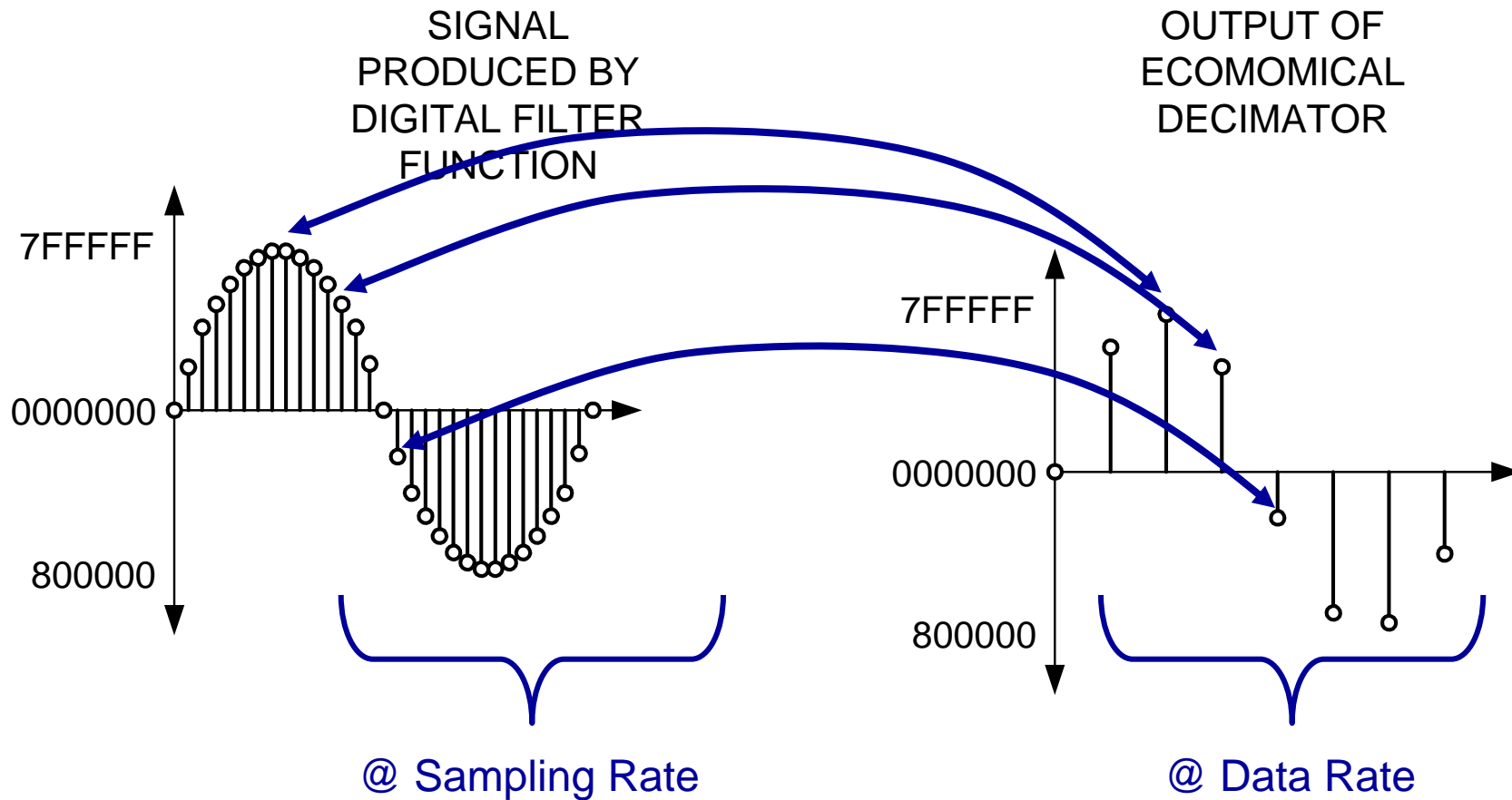
Decimation Digital Filter



Decimator Function: Averager

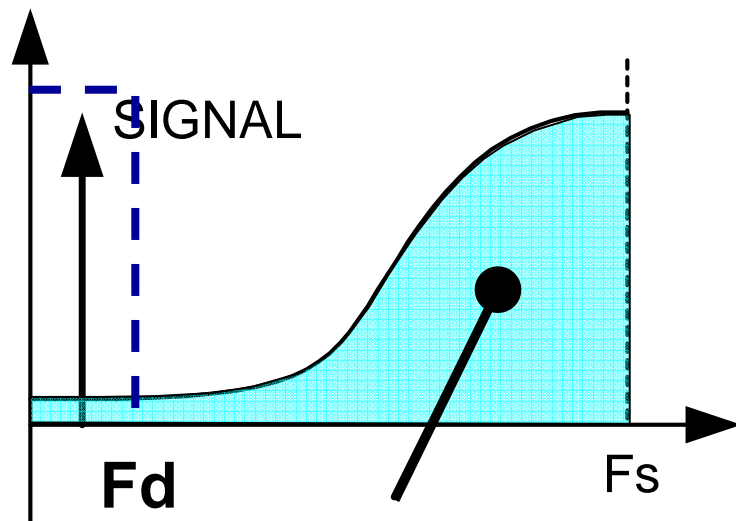


Decimator Function: Pick & Dump



Sampling speed vs. SNR

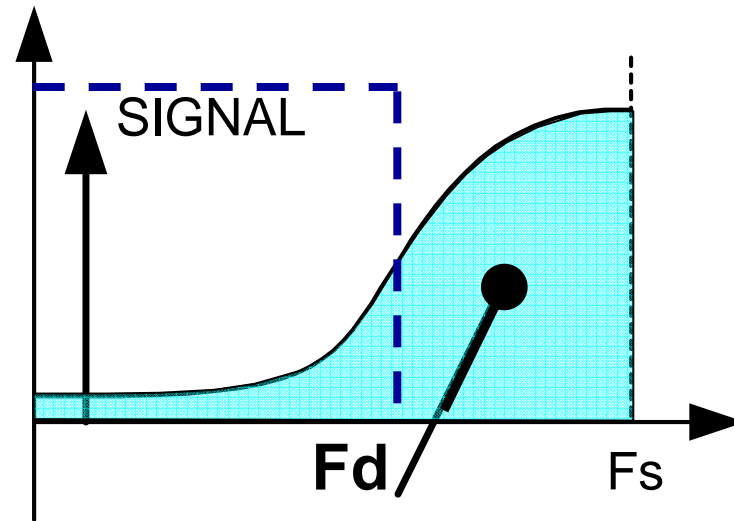
$$F_s / F_d = DR = K$$



QUANTIZATION
NOISE

A.

$$DR_A > DR_B$$



QUANTIZATION
NOISE

B.

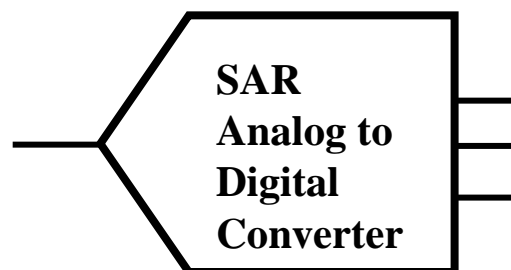
Additional Features

$\Delta\Sigma$ s often have additional features for data acquisition

- Analog PGA (ADS1282, ADS1248/7/6, ADS1230/2)
- Input Buffer (ADS1222/4/5/6, ADS1245, ADS1259)
- Burnout Current Sources (ADS1243/44)
- Multiplexers (most ADS12xx)
- More complete system solution (ADS1248, ADS1115)
- Sensor Excitation (ADS1248/7)

The SAR ADC

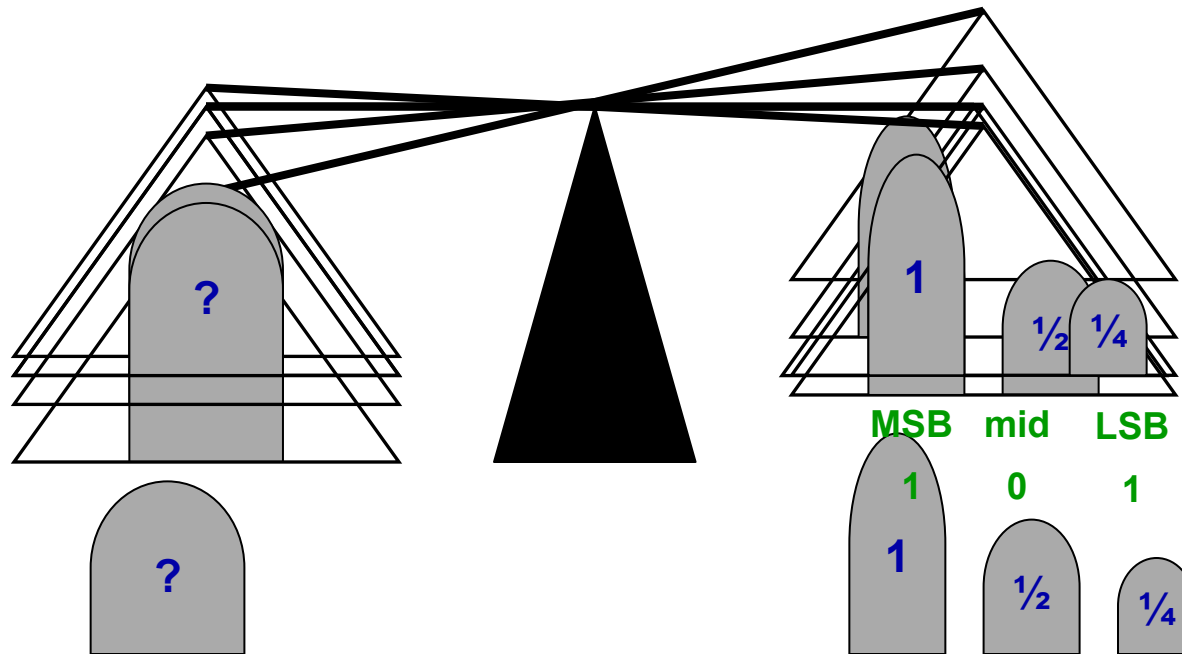
- Most Serial ADCs are SARs or Delta-Sigmas
- SARs are Best for General Purpose Apps
 - Data Loggers,
 - Temp Sensors,
 - Bridge Sensors,
 - General Purpose
- In the Market SARs
 - Can be 8 to 18 bits of resolution
 - Speed range: > DC to < 5 Msps
- SARs found as
 - Stand-alone
 - Peripheral in Microcontrollers, Processors



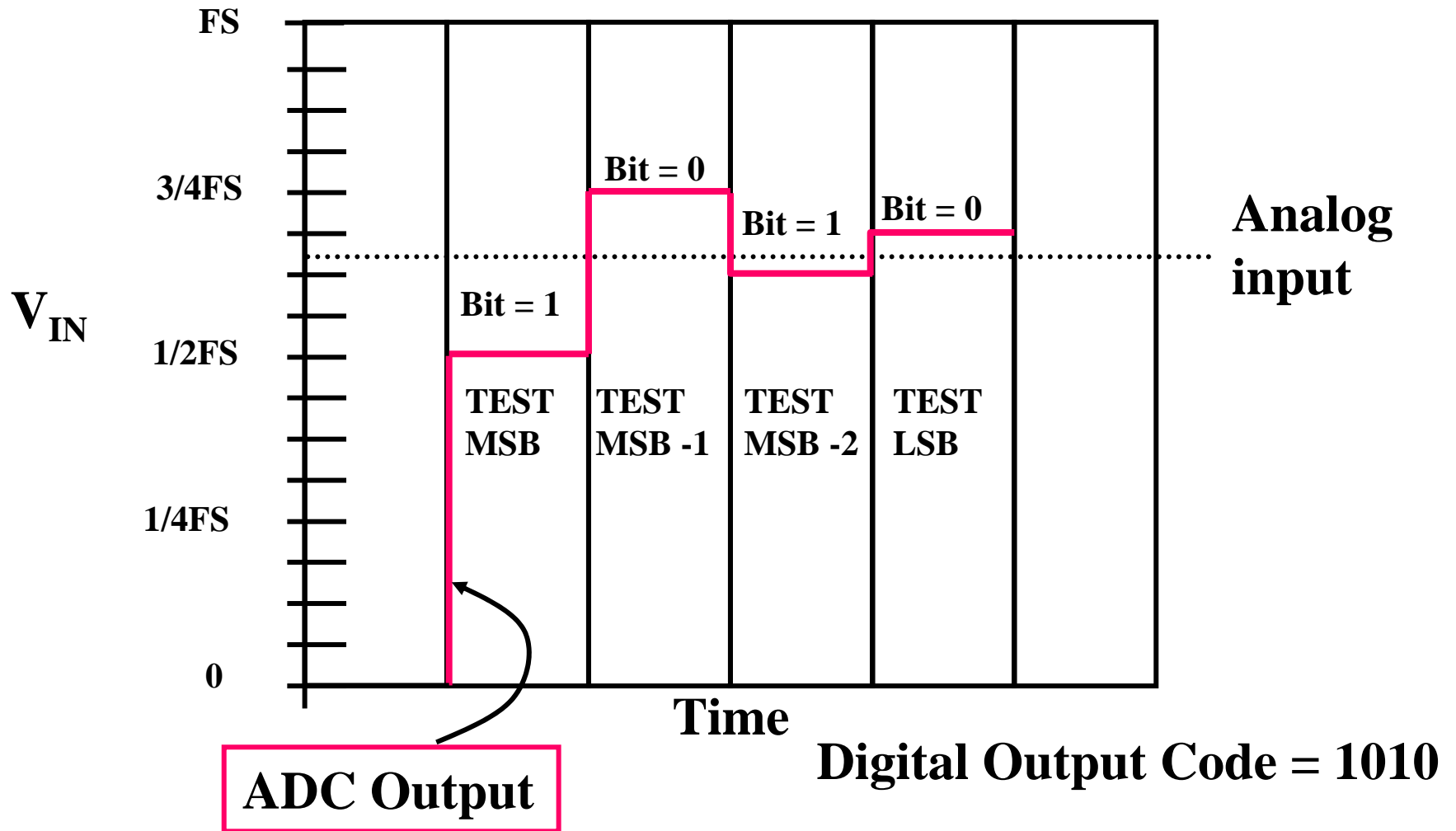
How Does a SAR work?

- Similar to a balance scale

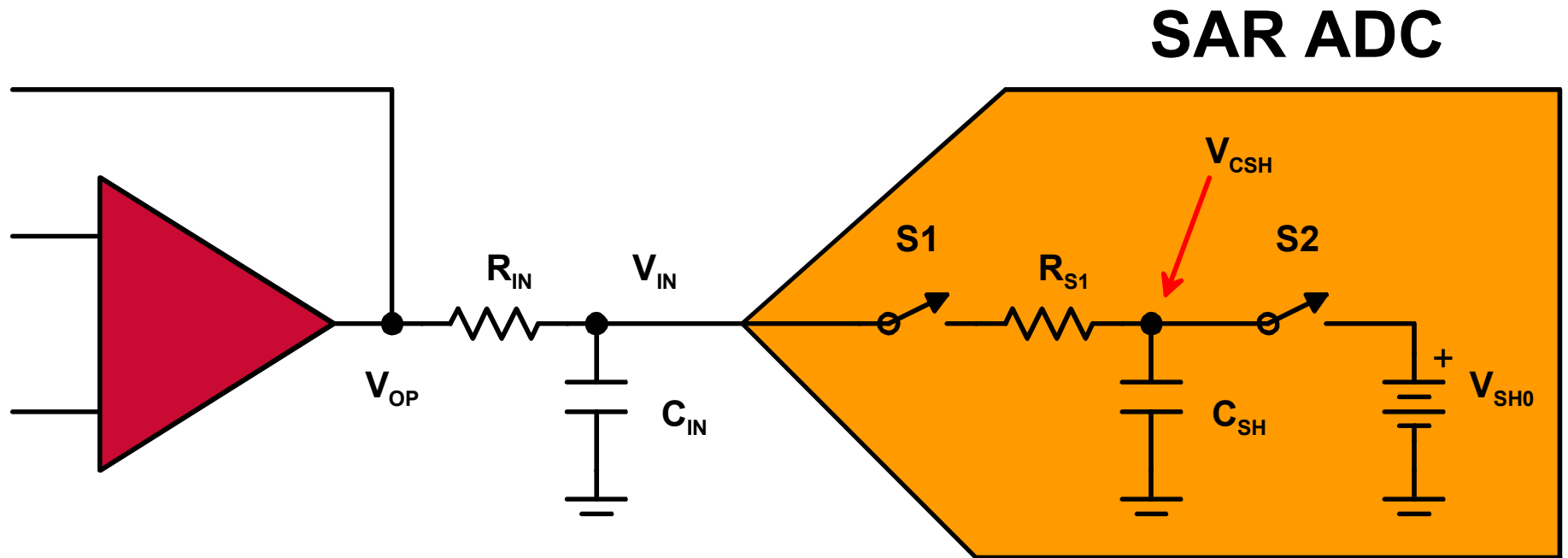
the MSB is determined first



SAR Conversion Concept



SAR Converter – Input Stage



Note: All capacitors must be able to charge to $\frac{1}{2}$ LSB within the acquisition time!

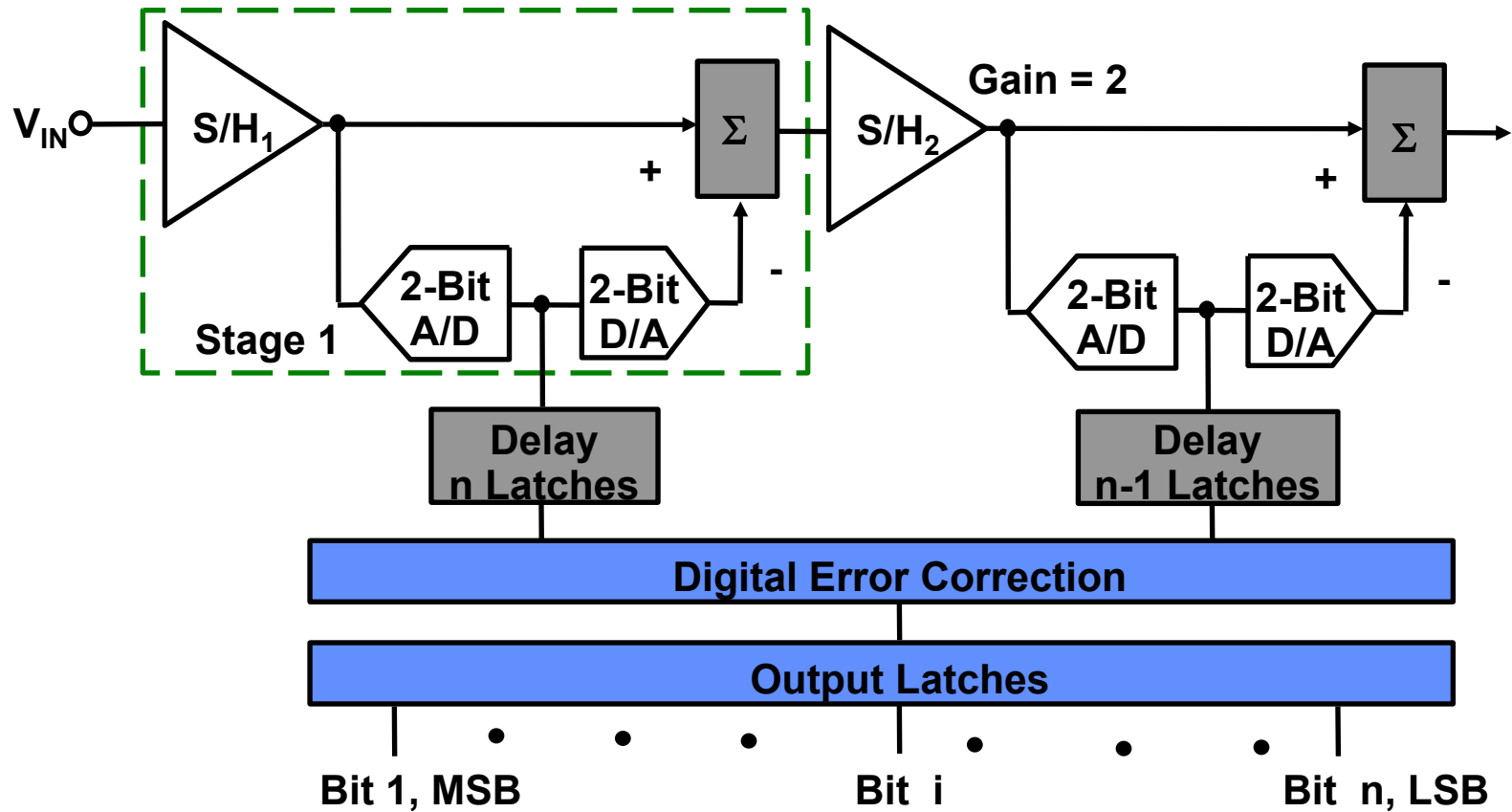
Additional Features

- Fewer options with SARs
 - Some converters have multiplexers (ADS82xx)
 - References (ADS78xx, ADS84xx, ADS85xx, etc.)
 - Input Buffers/Drivers (ADS8254/55/84)
 - PGA (ADS7870/71)
 - Programmable Alarm Level Comparator (ADS795x)

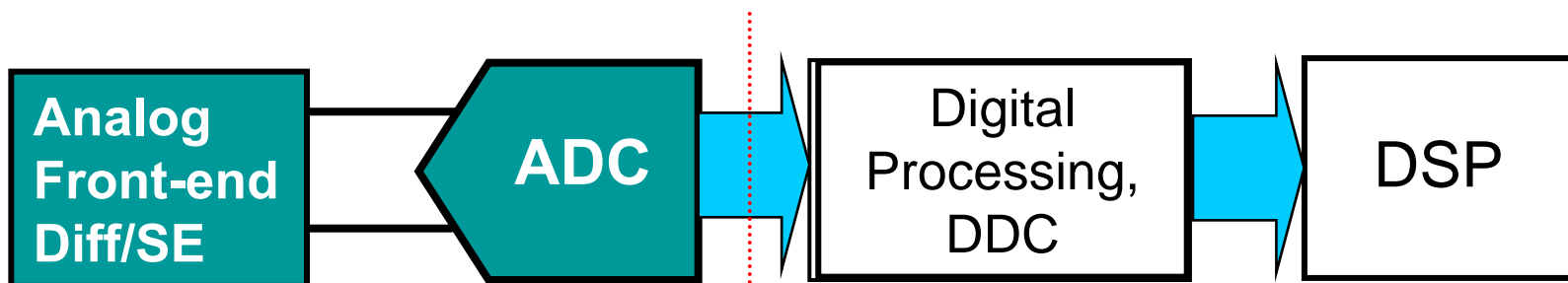
High Speed – Pipeline Topology

- Pipeline converters fit high-speed applications (5 MHz to >100MHz).
- Applications where you typically find pipeline converters are:
 - Wireless and Line Communications
 - Test and Measurement, Instrumentation
 - Medical Imaging
 - Radar Systems
 - Data Acquisition

Pipeline A/D Converter Architecture Overview



System



Signal Conditioning
Bandpass Filtering
Gain to Match FSR of A/D
SE to Diff Conversion
DC-level shifting

Conversion
digitization
mixing (alias)

Analog

Digital Processing
Frequency Translation
Decimation
Processing Gain (SNR)

Digital

DSP

What's the Application?

Time Domain

- **Imaging (CCD)**
 - Camcorders
 - Digital Cameras
 - Scanner
 - RGB/Comp. Video
 - Test Instrumentation
 - Medical
- **Important Specs:**
 - SNR
 - Slew-Rate/ tset
 - DNL
 - DC-Accuracy/ Drift

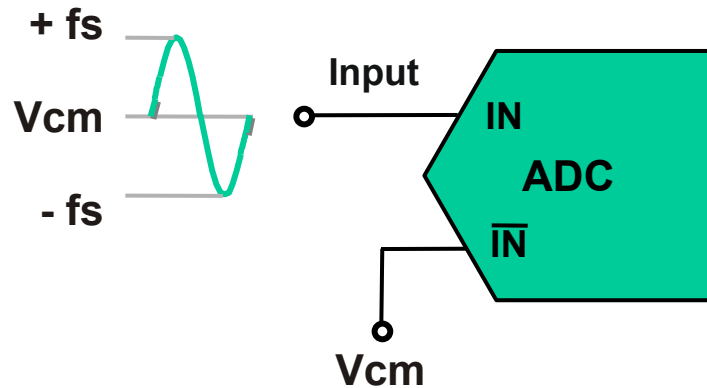
Frequency Domain

- **Communications**
 - Set-Top Box
 - Cable Modem
 - Basestation
 - IF Digitizer
 - GPS
 - Frequency Synthesizer
- **Important Specs:**
 - SFDR
 - ENOB
 - Analog Input Bandwidth
 - Jitter

ADC Interface Solutions

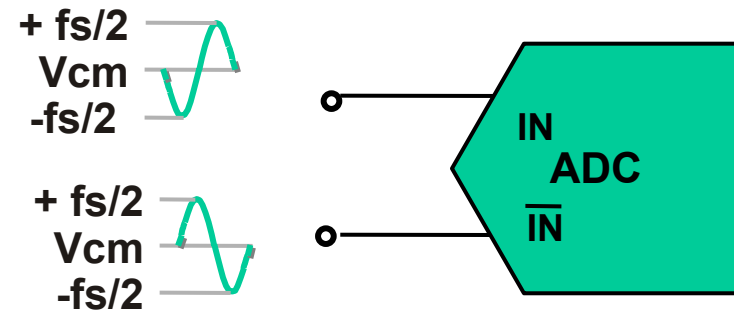
Principle Configuration Choices

Single-Ended Input (SE)



Requires full input swing from $+fs$ to $-fs$
 2x the swing compared to differential
 Input signal at IN typically requires a
 common-mode voltage for bias
 Input IN also requires a V_{cm} for correct
 dc-bias

Differential Input (DE)

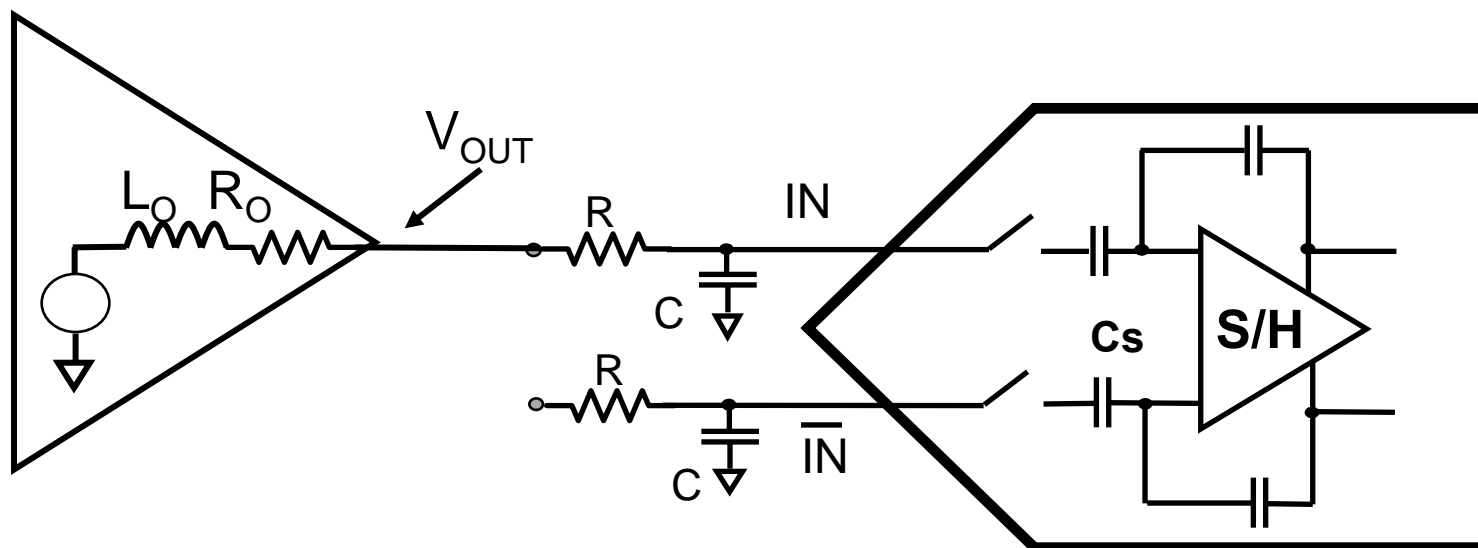


Combined Differential inputs result in
 full-scale input of $+fs$ to $-fs$
 Each input only requires 0.5x the
 swing compared to single-ended
 Both inputs require a V_{cm} for correct
 dc-bias

SE vs. DE Issues

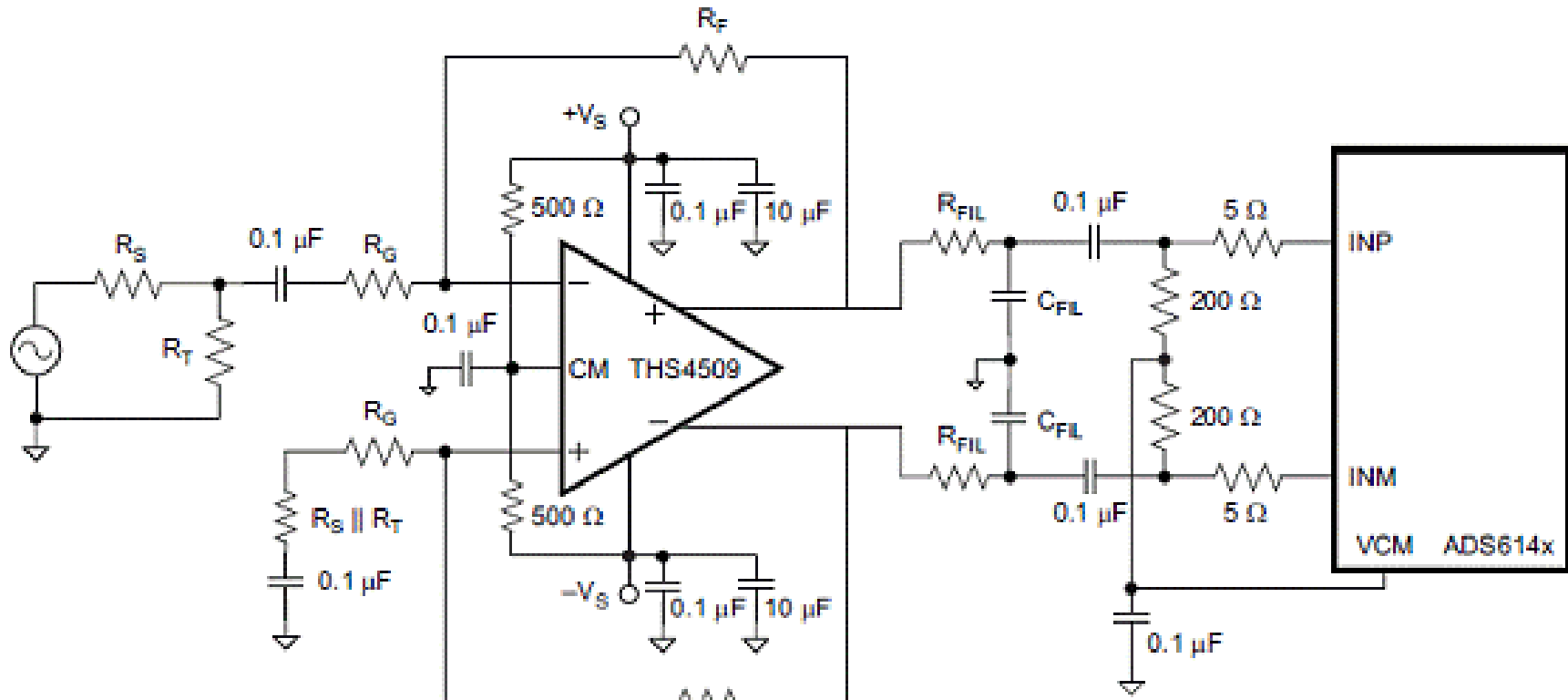
- Single-ended Inputs (SE)
 - Degraded dynamic performance (larger FSR)
 - Common-mode voltage and op amp headroom may limit use for dc-coupling
 - Best suited for Time Domain applications
- Differential
 - Optimized performance due to lower FSR, Reduction of even-order and common-mode components
 - Best for higher input frequencies (IFs)
 - More complex driver circuitry (consider Diff – Amps)
 - Best suited for Frequency Domain applications

Driving Capacitive Input ADCs



- Due to Opamp's finite (R_O) output impedance, V_{OUT} will drop momentarily when cap load is switched.
- As the output recovers, ringing may occur, which results in increased settling time.
- Use external R : isolates OpAmp output from capacitive load and improves settling.

Differential ADC Driver



Driver Solution:

- No Transformer
- VCM matched to ADC
- Good even-order harmonic rejection
- Easily configured for gain and low-pass filter

Choose the right A/D converter for your application

What do you know about your signal?

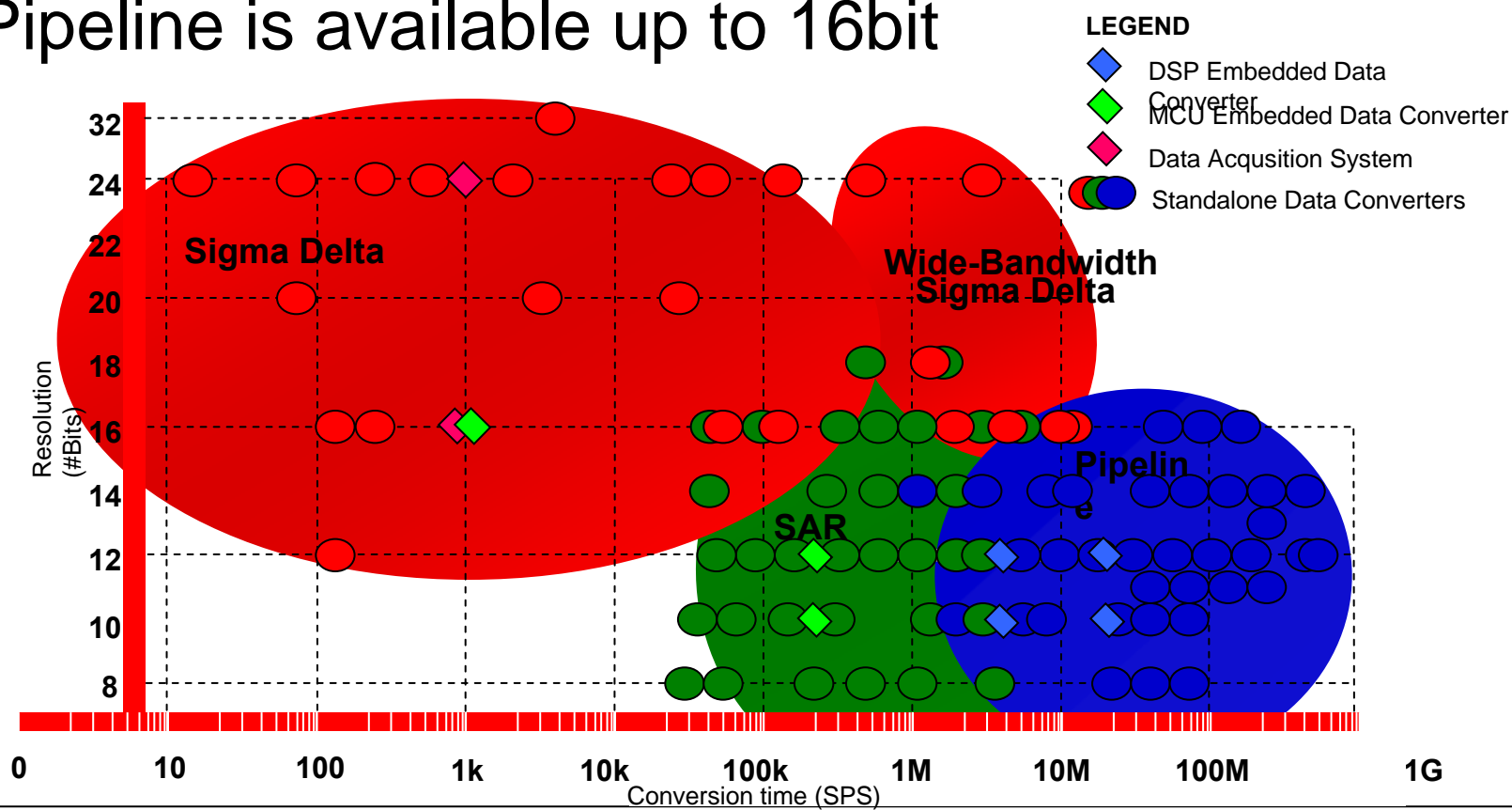
- Desired Bandwidth?
 - up to 4MSPS SAR,
 - up to 10MSPS Delta Sigma,
 - above Pipeline
- Is DC precision important?
 - YES -> look at Delta Sigmas at first choice
 - alternative SAR Converters with DC Precision
- Does your signal have frequency content above Nyquist?
 - YES and it needs to be detected -> SAR or Pipeline with external Bandpass Filter
 - YES but can be ignored -> SAR or Pipeline, or Delta Sigma with Sinc Filter and an external Anti Aliasing Filter (AAF)
 - YES, but no external filter possible -> Delta Sigma with FIR
 - NO -> Delta Sigma with Sinc or FIR filter or SAR or Pipeline

What do you need to find out about your signal?

- A specific point in time needs to be frozen?
 - YES -> Sample and hold Stage is needed like in SAR, Pipeline (no Delta Sigma)
- Can an average of your signal be used as long as the constant phase relation does exist?
 - YES -> Delta Sigmas can be used as they average the signal
- Do you need to convert multiple signals in phase relation to each other?
 - YES -> multiple synchronous S/H are needed or synchronous Delta Sigma Modulators – Multi Channel converters exist for all three types SAR, Delta Sigma, Pipeline
 - NO -> Multiplexing can be used. Exists for SAR and Delta Sigma.

Desired resolution?

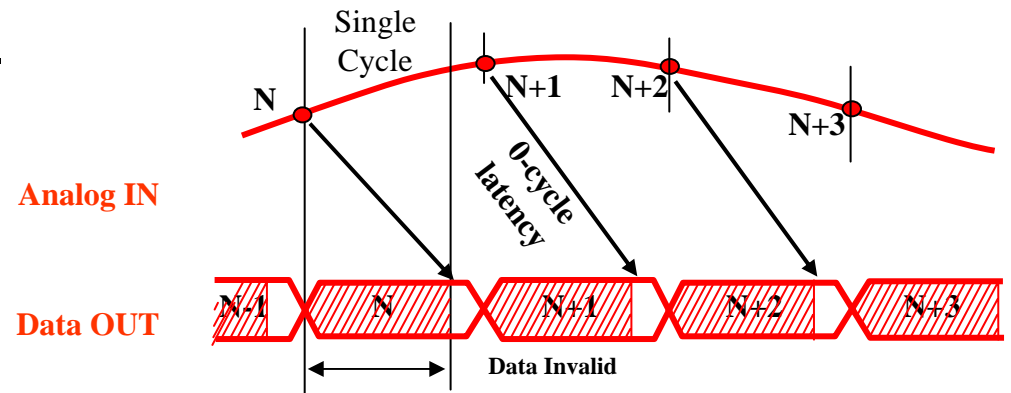
- SAR is available up to 18bit
- Delta Sigma is available up to 24bit
- Pipeline is available up to 16bit



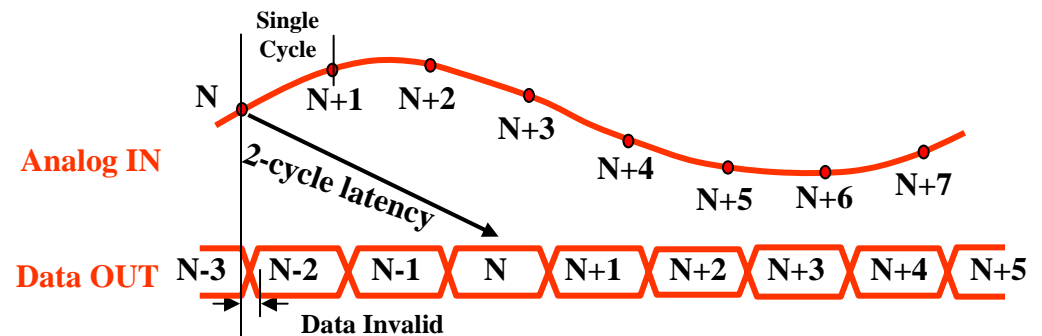
Is a latency tolerable?

Is the measured signal information needed immediately or can a delay be tolerated as long as it is constant?

- Immediate -> SAR or pipeline & high speed serial or parallel interface
-> 0-cycle latency,
1 Fdata delay



- Delay -> Delta Sigma with 2-5 Fdata delay using SINC filter with serial interface SPI/I2C



- Huge delay -> Delta Sigma with multiple Fdata Delay from FIR with linear Phase (number of TAPS/2), e.g. 78 Fdata delay

Strengths and definition of Linearity

- SARs have good monotonicity
spec: INL / DNL
- Delta Sigma is monotonous by principle
spec: THD
- Pipeline: due to the staged architecture (ADC-DAC-ADC...) non-linearities add-up
spec: SFDR

Input voltage range?

- Does it fit directly to an available ADC?
 - single ended or differential inputs exist
 - SAR ADCs offer unipolar or bipolar
 - Delta Sigmas offer unipolar and bipolar, can have build in PGA
- Can it be adapted externally by OPAs / INAs / resistors?
 - Sometimes external driving circuit is needed anyway
 - SAR and Pipeline: signal can be adapted with this for saving cost and power
 - Consider signal conditioning in combination with single supply converter

Power consumption

- Power consumption and/or dissipation is generally a concern, but performance needs may demand certain power
- Delta-sigma: allows nice trade-off between resolution, speed and power-consumption
- SARs: are generally the low-power option
- Pipeline ADCs: are relatively power-hungry to achieve their high performance-levels

Agenda

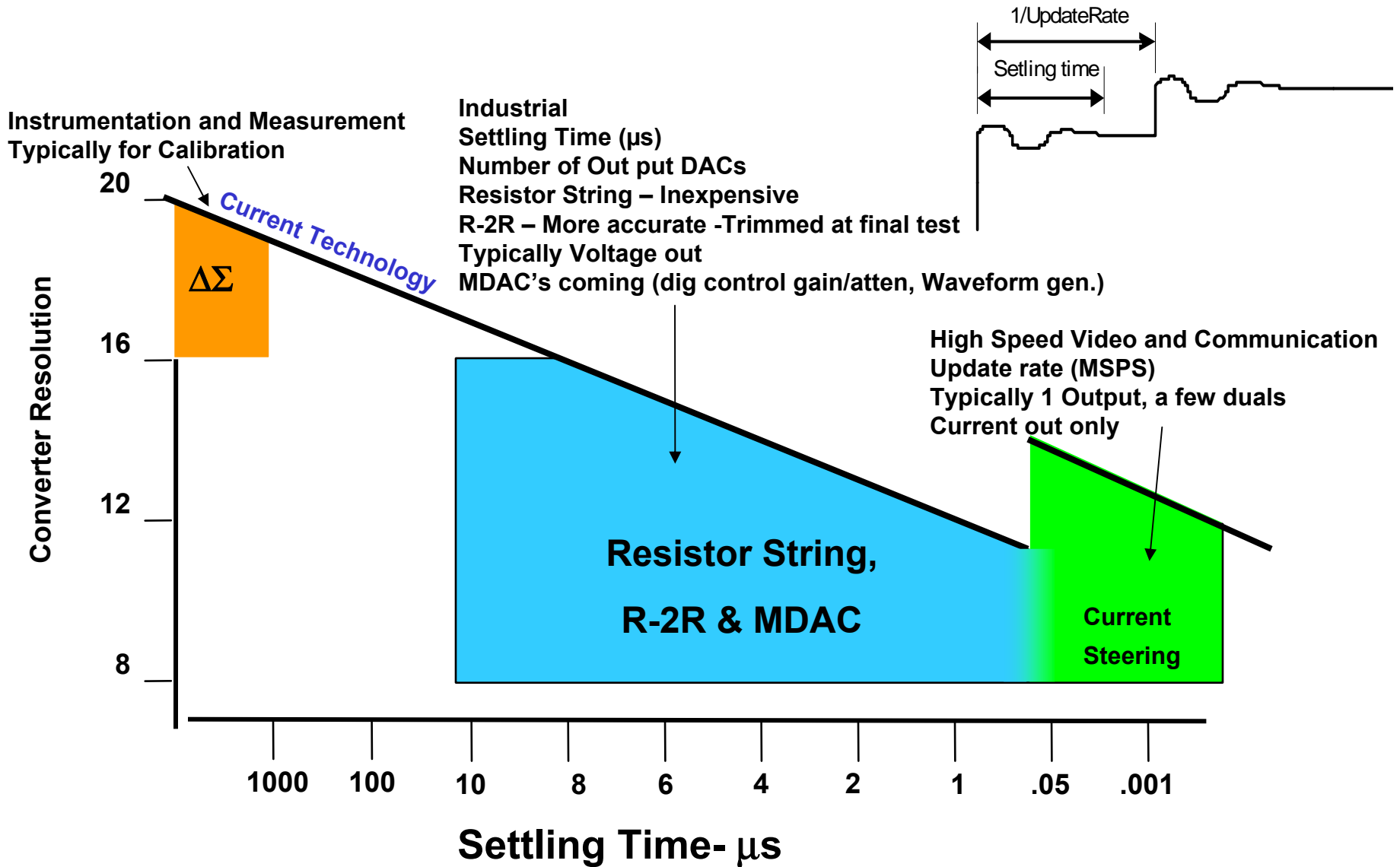
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 - High-Speed Current-Steering DACs

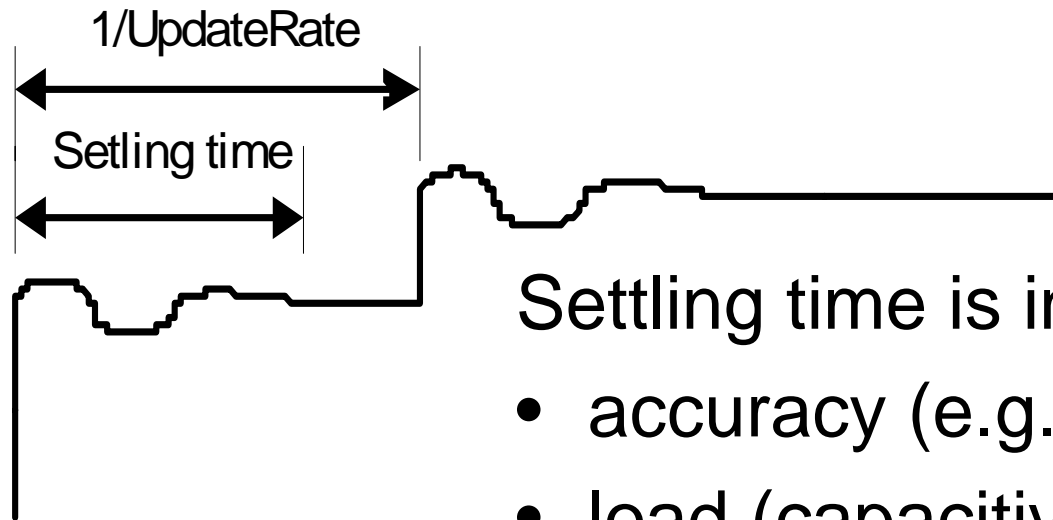
DAC Architectures

- R-2R—The oldest and still the “cleanest” conversion method
- String—A tapped resistor string
- Delta Sigma—(One bit) Trades resolution in amplitude for resolution in time. Requires a system clock that is faster than the bit data

TI DAC Technologies



Settling time definitions

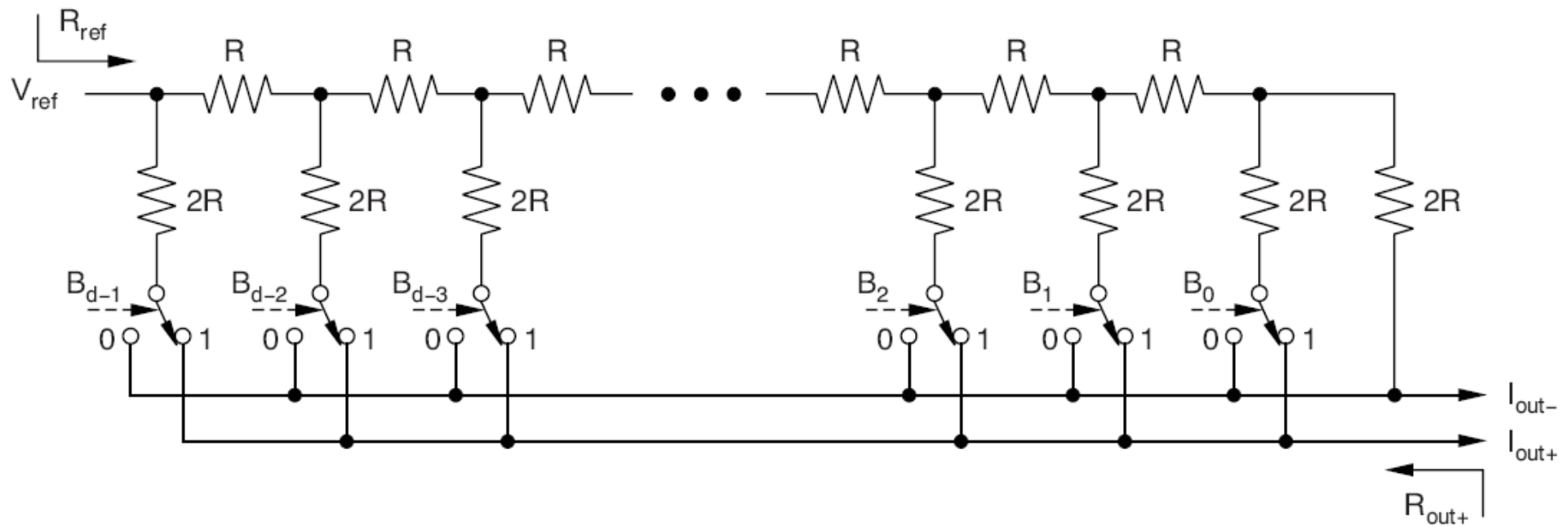


Settling time is influenced by

- accuracy (e.g. 0.003% or 0.1% FS)
- load (capacitive, resistive)
- Digital Code step size

DAC9881 (18b, 5us)	Settling time	To $\pm 0.003\%$ FS, $R_L = 10k\Omega$, $C_L = 50pF$, code 1000h to F000h
DAC8564 (16b, 10us)	Output voltage settling time	To $\pm 0.003\%$ FSR, 0200h to FD00h, $R_L = 2k\Omega$, $0pF < C_L < 200pF$
		$R_L = 2k\Omega$, $C_L = 500pF$
DAC5681 (16b, 1GSPS)	$t_{s(DAC)}$ Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF

R-2R or Current Segment Topology



This classical approach delivers a current mode output.
For voltage mode output, this structure is followed by an I/V converter

Advantages of R-2R DACs

- Can achieve high performance INL & DNL
- Medium Settling Time Capability
- Low Noise R-2R Ladder

Disadvantages of R-2R DACs

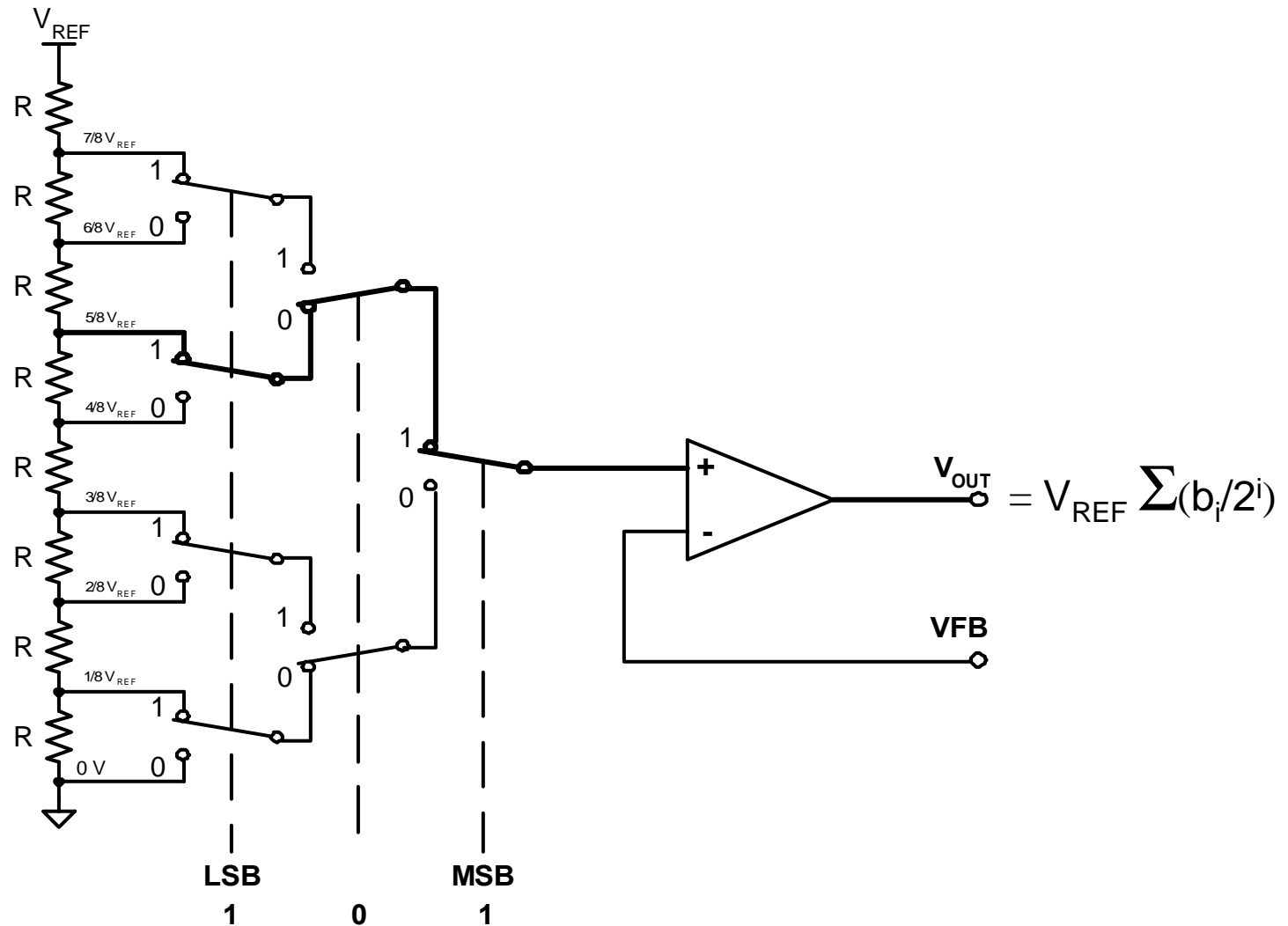
Data timing skews

- causing high output glitches
- Need HV transistor input stage for HV DAC Buffer → Low Bandwidth & Settling
- Internally, requires high common mode voltage swing output amp

Applications for R-2R DACs

- Automatic test equipment
- Precision Instrumentation
- Industrial control
- Data Acquisition systems
- Control Loop systems

Principle Resistor String DAC Architecture



What is a Resistor String DAC?

- It is basically built with the following:
 - A voltage reference.
 - A set of matched resistors.
 - A set of switches.
 - And an output buffer.
- Control and interface logic, and all other features varies upon design specifications.

Advantages of String DACs

- Inherently monotonic
- Cost Effective
 - Simple to build (by design)
 - No need for trimming
- Low Glitch Energy
- Good DNL performance

Disadvantages of String DACs

- Requires $2^N - 1$ matching resistors
 - Resolution is limited
 - Size can grow with resolution requirement
 - High resolution is achieved by pipeline-like architectures which compromises monotonicity
 - Decoding logic
 - Many interconnections
 - Requires output buffer
 - Accuracy (due to linearity errors)
- } These factors limit the achievable speed of the DAC

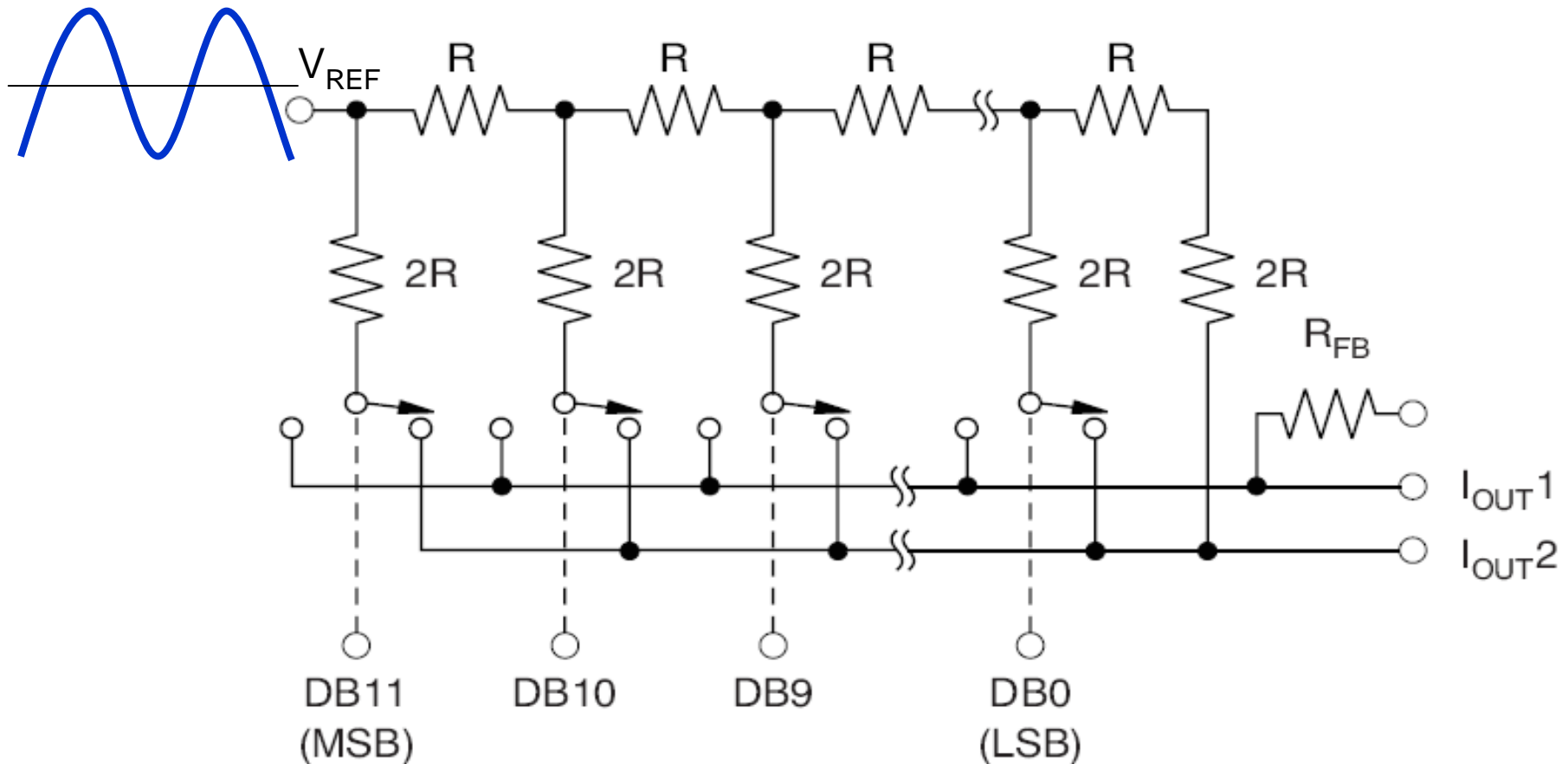
Applications for String DACs

- Control Loops
 - Industrial Control
 - Digital Servos
 - Machine and Motion
- Trimmers
- Instrumentation
- Digital Offset and Gain Adjustment

String DACs – Not-recommended Applications

- High Speed Applications
- Communications
- Signal Waveform Generation
- Precision Voltage Setting

Multiplying DAC Architecture



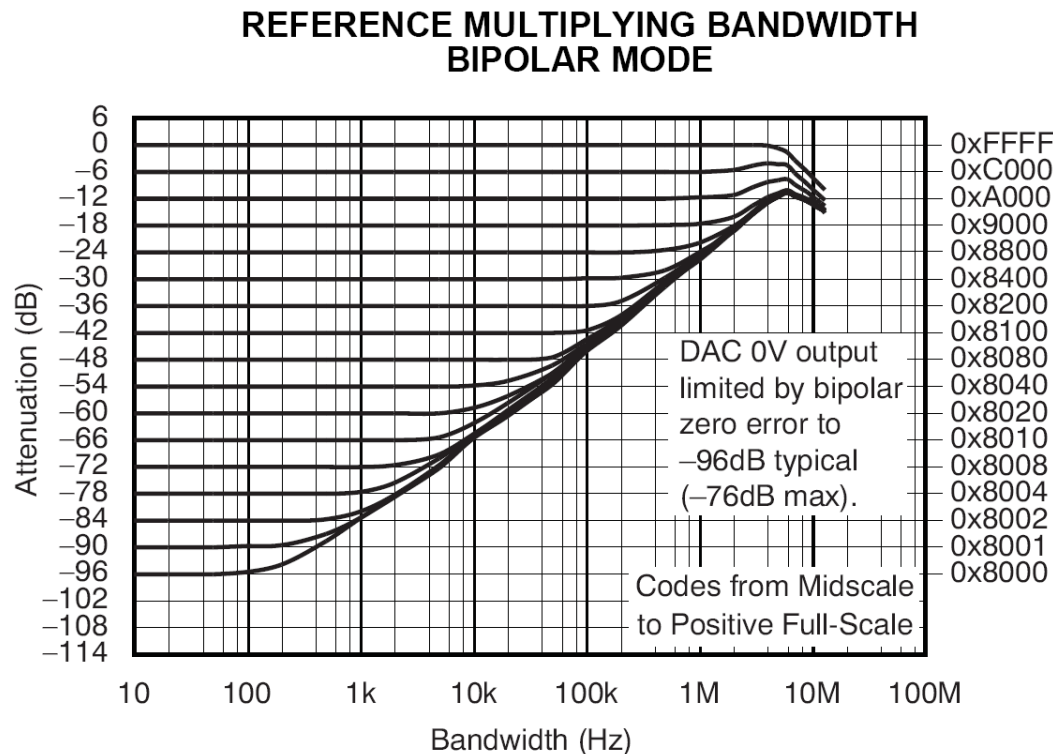
The above structure is essentially a R-2R-architecture. The “invisible” difference is , that V_{REF} can be an analog signal, i.e. an alternating signal, even crossing zero Volts.

Multiplying DAC

- Output Amplifier functions
 - Output Amp I/V: Common Mode Voltage @ Fixed 0V
 - High Voltage (HV) capable with external HV-OPA I/V
 - High Bandwidth Capability
- MDAC internal characteristics
 - Can achieve high performance INL & DNL
 - Reference-current is constant
 - Low noise R-2R ladder
 - Flexible reference input (Zero-Crossing, AC-signal)

MDAC – what is it used for?

- Programmable Attenuation (fixed digital input, reference used as signal-input)



DAC8822: attenuation vs. reference multiplying bandwidth at various digital codes

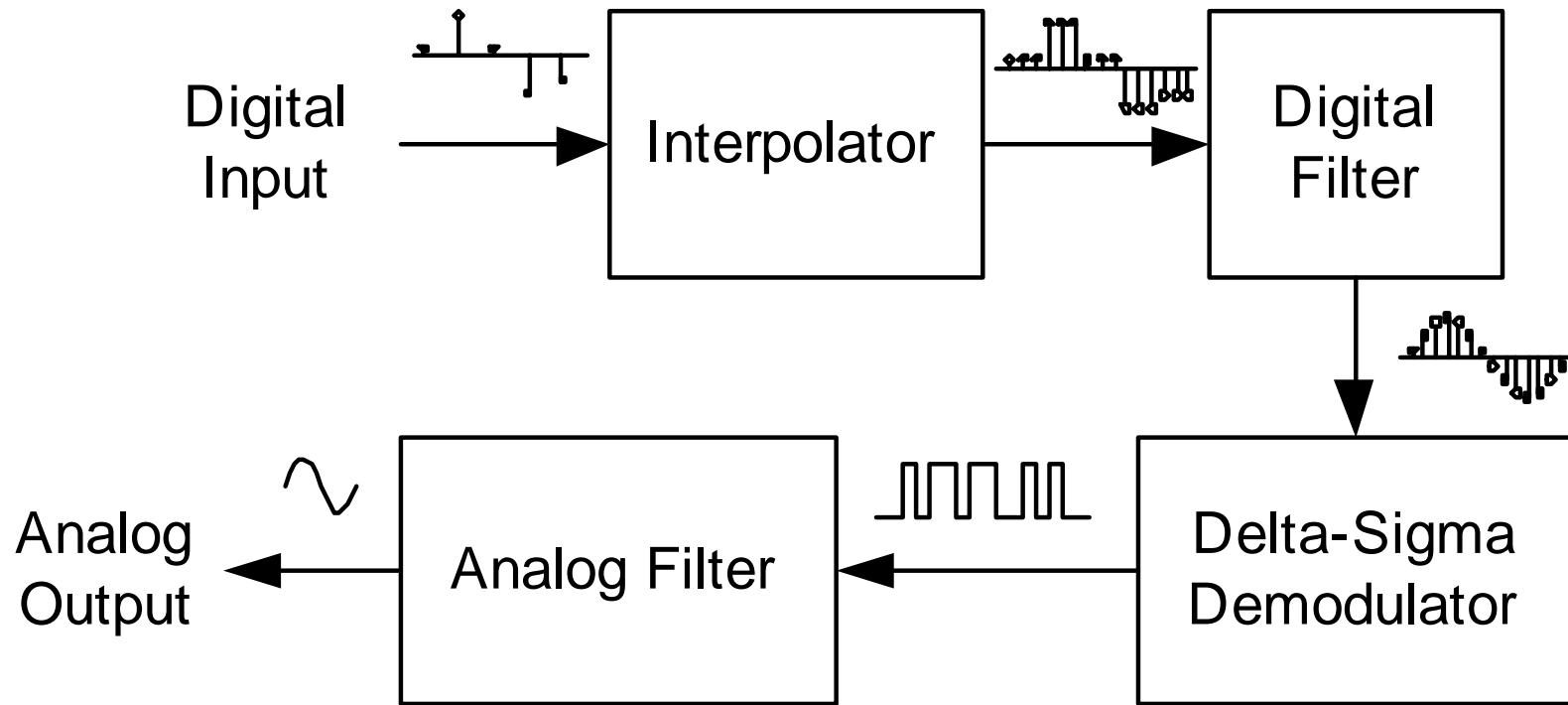
- Selectable Inversion (by inverting the reference)

Multiplying DAC

Appropriate applications

- Waveform Generators
- Audio-Applications
- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration
- Industrial Control PLCs

Delta-Sigma DACs



A Delta-Sigma-DAC is basically an DS-ADC operated in reverse direction: Oversampling of the digital input, digital filtering, demodulation, analog filtering. Predominantly used in Audio-DACs.

Delta-Sigma DAC Properties

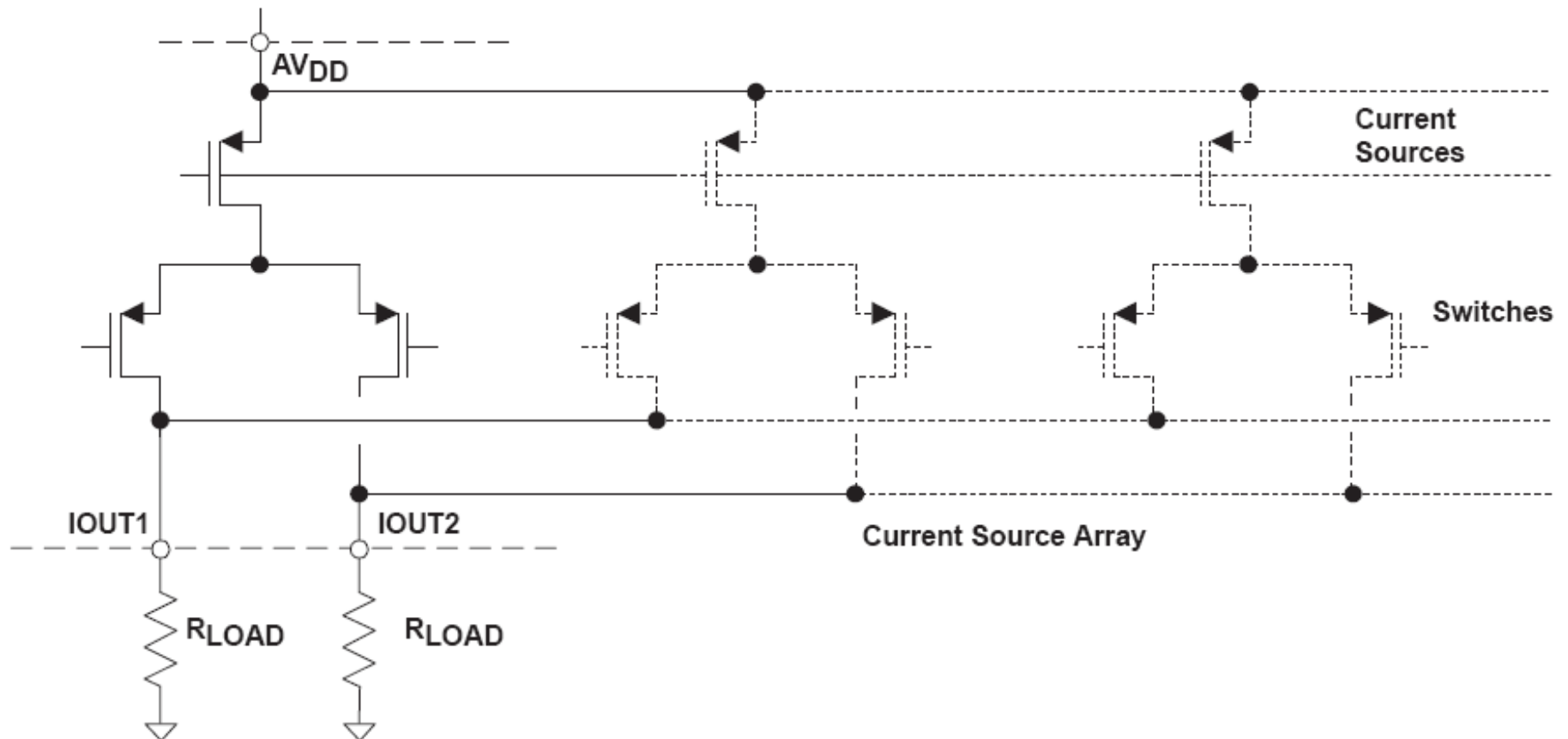
- High resolution
- Low Power
- Voltage output
- Good Linearity
- Low Cost
- In Audio: moving noise out of audible range

- Settling time ~2ms
- Long Latency
- Not optimized for DC

Delta-Sigma DAC Applications

- Audio-Applications
- Sonar
- Process Control
- ATE Pin Electronics
- Closed-Loop Servo Control
- Smart Transmitters
- Portable Instruments

Current steering DACs



Current steering DACs replace the resistor arrays of R-2R-DACs with weighted current sources

Current steering DAC Properties

- Highest speed (1 GSPS+, 10ns settling time)
- Best AC-performance
- 20mA output current (typ)
- Low complexity, low glitch-energy

- Current output: often I/V-converter or transformer required

Current steering DAC Applications

- Communication Infrastructure
(Wireless and Line Communication)
- Test Equipment
- Radar

Choose the right D/A converter for your application

Desired resolution and settling time?

- Resolution
 - R2R available up to 18 bits
 - String available up to 16 bit
 - Delta Sigma available up to 24bits (Audio DACS <32bit)
- Settling time
 - Note the differences in definition!
 - What update rates / output frequencies are available?
 - 16 bit -> 1GSPS
 - 18 bit -> for DC-precision
 - 24 bit -> 768kHz (Audio)
 - 32bit -> 192kHz (Audio)
 - Consider over sampling for relaxing the reconstruction filter requirement

Linearity and Glitches

- Linearity
 - INL, DNL for R2R and String
 - R2R is trimmed, offers very good linearity but high cost
 - String: fair linearity low cost
- Does output glitch energy matter?
 - go for String DACs for lowest glitch
 - some R2R are pretty good but not as good as String DACs

Integration and Interface

- Multiple outputs
 - 2ch, 4ch, 8ch DACs with synchronous output update
- Reference source?
 - Internal or external fixed Vref
 - External Vref can be variable -> multiplying DACs
- Interface
 - Serial, Parallel, SPI, I2C or High Speed LVDS

Output voltage range?

- Consider using external Opamps to gain and level shift the output signal – it can save cost in combination with a single supply DAC
- Some DAC have current outputs anyway and a trans-impedance stage is required

Power consumption

- Power consumption and/or dissipation is determined by the output impedance and drive-strength rather than architecture
- Precision DACs usually have 10kOhm impedance and drive 1mA, i.e. 10mW @ 10V.
The current is drawn from the reference, hence DACs with internal REF have higher consumption
- Current-Steering DACs for high-speed applications drive 20mA and consequently require higher supply-currents.